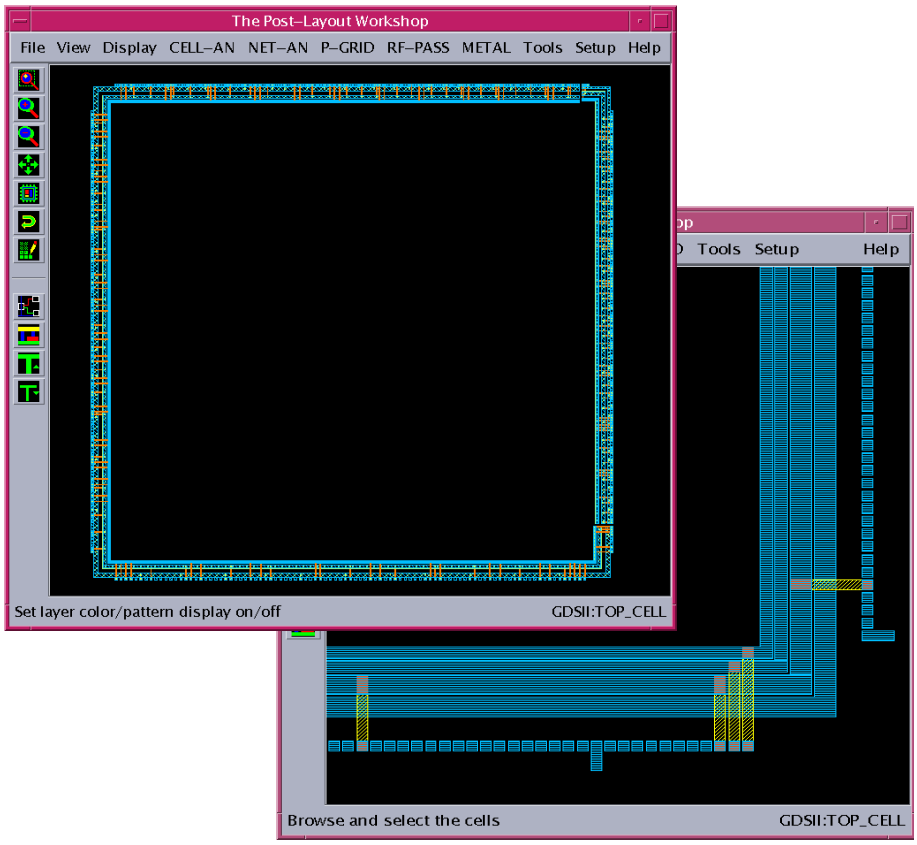
RING Designer

VLSI Power Distribution Ring Design Tool



RING Designer™ Features:

- *Solves the problem of generating accurate Spice decks to analyze IO rings with packaging effects*
- *Helps with optimization of power pin placement and complex IO ring designs*
- *Analyzes potential ground bounce and simultaneous switching noise problems*
- *Analyzes and assists in balancing current loads to I/O pad and voltage input pads*
- *Fast what-if iterations taking only minutes each*
- *Includes all ring and packaging parasitics with input from OEA NET-AN, METAL, and HENRY*

RING Designer is an easy to use tool for optimizing the design of VLSI power distribution I/O rings. Common problems of ground bounce and simultaneous switching noise are easily debugged and solutions found by fast turn around what-if analysis. RING Designer allows for fast changes in ring width, pad locations, by-pass capacitor value selection and location, and buffer size selection and locations to resolve problems.

Full SPICE Analysis of Ring Circuit

RING Designer allows the user to easily specify the full SPICE circuit parameters of the planned ring design including I/O buffer SPICE circuits, power ring sizes, and locations of by-pass capacitors, voltage supply pads and I/O buffers. Using the OEA 3D Extraction tool a full RCLM SPICE circuit of the ring is created. Also, package parasitics and PCB parasitics can be extracted using the OEA HENRY and METAL programs. Once the complete circuit is specified, SPICE is run and the resulting transient analysis is given for various switching vectors.

Eliminates Over Design

By calculating the optimal number of VDD/VSS supply pads, RING Designer can save package pins and even allow a smaller pin count package to be used in some cases. Cost trade-offs are made easily because the PCB, package and chip rings are modeled together.

OEA International, Inc.