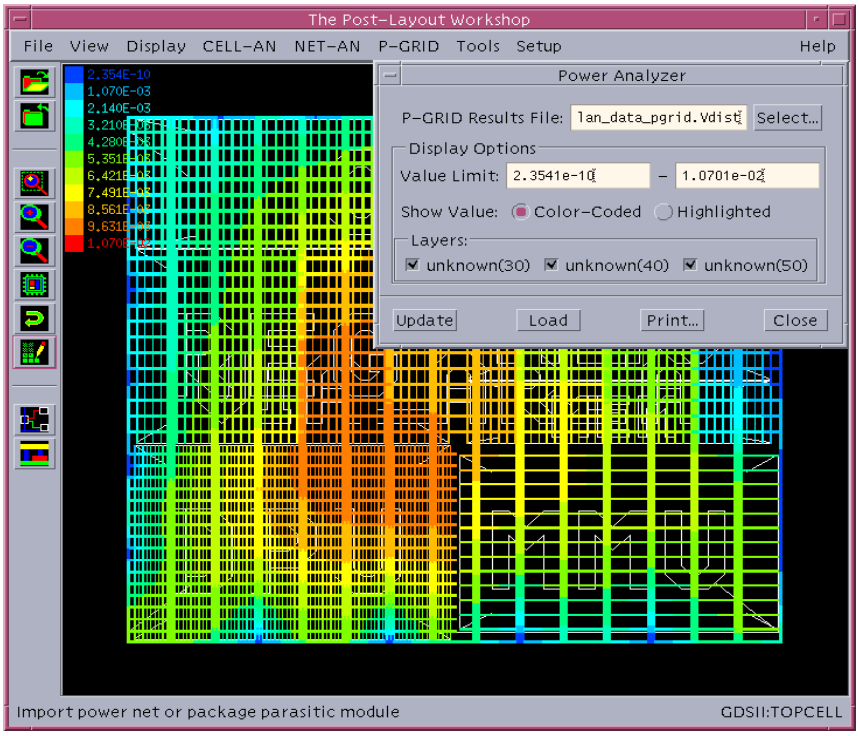
P-GRID

3D Power Net Analysis Design Tool



P-GRID™ Features:

- *Utilizes full 3D field simulation solver to generate high accuracy distributed network*
- *Flexible voltage source definition as point sources or automatically assigned at defined edges of block routing*
- *Flexible current source definition by area with automatic node pickup or with user specified point sources*
- *Graphical reporting of violations on layout for easy correction*
- *Color-coded mapping of current, current density and voltage drop*
- *Custom formatted violation reports*
- *Optional automatic addition of phantom metal and vias to represent top layer routing on blocks*
- *Push-button graphic interface or batch operation*
- *Runs on all popular workstation platforms*

In today's high performance VLSI designs, accurate extraction and modeling of the power and ground distribution network is essential. P-GRID employs a fully seamless 3D Laplace/Poisson field solution using the fast proprietary "Cheetah II" solver to extract distributed current flow model for even the most complex networks. Other 2D and square count based net extraction methods do not accurately account for the 3D current distribution and current crowding effects. Also, because the results of other tools extraction may just be a SPICE deck, it can be difficult or impossible to use because of too many I/Os or a SPICE deck just too large to be simulated. Thus, results derived from these 2D tools can be inaccurate or impossible to use. P-GRID will simulate the average IC block power net, solving in excess of 50 million equations, in just minutes on popular workstation platforms.

Hierarchical Full Chip or Block Level Simulation

When designing a chip, individual blocks are often given to different design teams. P-GRID can be used during the block design process to assure the correct power distribution network design at the block level. With block level current distributions saved, it can then be used at the full chip level to analyze top level power distribution network interconnects.

Easy Voltage Source Definition

P-GRID automatically finds edge voltage source points from user defined block edges and layers. Or, if one knows the exact voltage source points, these may be defined and utilized by P-GRID without interpolation.

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Block or Specific Current Source Definition
Many times, specific detailed switching current source information is not known or easily obtained. The average and worst case block current is however normally available to the designer. P-GRID is capable of utilizing either specific xy data or full block current source data. Block current is distributed through all contacts in the block on an area basis.

Graphical Output of Results
P-GRID accurately calculates voltage drop, current, and current density distribution at each via and metal segment in the entire network. For easy interpretation of this data, P-GRID displays an easy to read color-coded view of this distribution. This lets the user quickly discover and focus on areas which need correction.

Graphical Violation Reporting
P-GRID will allow the user to create a custom violation file for voltages below user supplied threshold voltages and current densities by layer above user defined values. With user supplied limits, locations of violations are flashed and values calculated at those locations.

Optional Top Layer Phantom Routing Created
Sometimes when simulating a block, the top layer distribution metal and vias are not yet routed. P-GRID allows the user to quickly add additional metal layers and automatically generates the maximum number of vias to the new metal crossover areas.

Connectivity-Based Graphic Interface
Reading standard GDSII data, display of the layout, building the 3D model, and graphic display of color-coded delays are accomplished with the most advanced and flexible IC graphics tool on the market today, Post-Layout WorkShop. Display variables such as colors, stipple pattern, layer priority and layer on/off display status are easily modified.

Other Related OEA Products

METAL - A general purpose 2D/3D interconnect simulator for extracting RCL parasitics from interconnect structures. It features automatic mesh generation and refinement, and automatic SPICE sub-circuit generation.

NET-AN - A three-dimensional IC multi-net analysis tool for extracting distributed RCLM SPICE networks from critical IC nets.

P-PLAN - A VLSI power distribution network floorplanning tool used with P-GRID for optimizing the geometric configuration of VDD and VSS rings, internal power rails, and ring voltage source pad locations using estimated block current sources.

SPIRAL - A design synthesis tool set for creating embedded spiral inductors, baluns and transformers in RFICs. It integrates together a geometry building engine, an optimizer, a 3D field solver for extraction of RCLM, and a frequency dependent circuit simulator. Outputs include GDSII, graphical plot file, SPICE models, and S-Parameter and Z-Parameter files.

BUS-AN - A tool for exploring the design space of a process technology as it relates to interconnect design limits and interconnect behavior. BUS-AN performs a variety of pre-design explorations such as inductive shielding effects, buffering strategies, clock-tree prototyping, and process corner simulations.

CELL-AN - A three-dimensional level SPICE extraction tool that generates a cell or macro sub-circuit with significant RC, S/D resistances, and geometry dependent transistor SPICE model parameters.

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