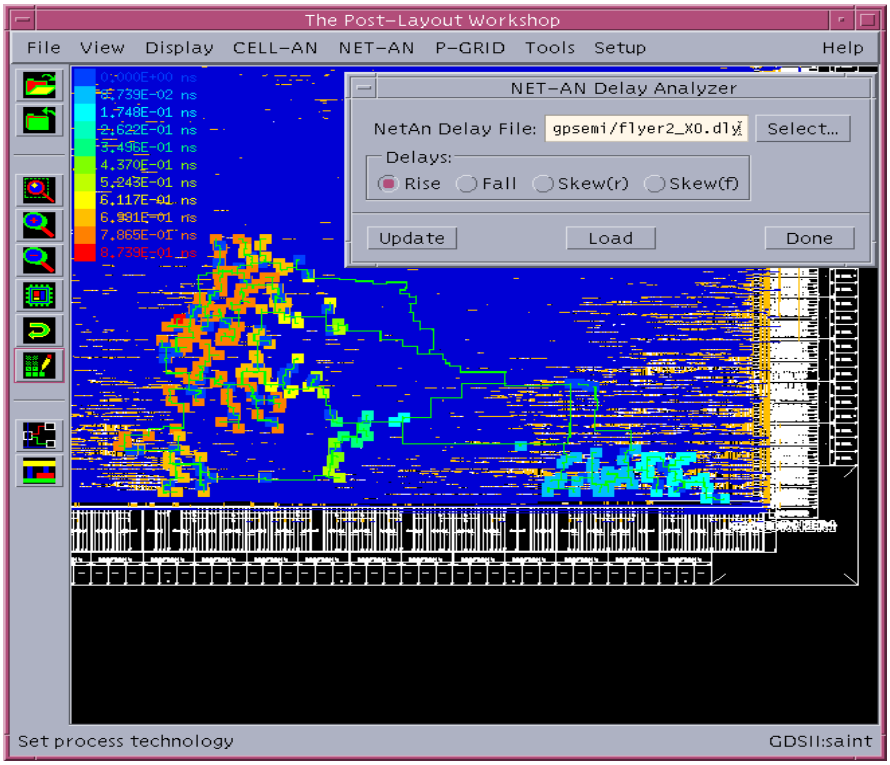
NET-AN

Multi-Net 3D Field Solver Extraction Tool



NET-AN™ Features:

- ***Full 3D seamless field solution for the highest accuracy***
- ***Distributed RCLM SPICE sub-circuit output***
- ***Extracts by net, tree, or path from custom, or cell based designs***
- ***Single or multi-coupled net extraction***
- ***Graphic display of delays***
- ***Automated LEF/DEF interface with an optional PrimeTime Interface***
- ***Graphic net or cell browser***
- ***Interactive graphics or batch operation***
- ***Fully integrated with popular EDA design flows***
- ***Runs on all popular workstation platforms***

In today's high performance VLSI designs, accurate extraction and modeling of critical interconnect paths, such as clock trees, bit, and word line paths is essential. NET-AN is the only true seamless 3D critical multi-net field simulator which takes into account the full 3D nature of the problem providing accurate simulation of even the largest and most complex nets. Other formula-based or cut & paste extraction methods do not accurately account for all of the 3D fringing parasitics, which are significant in deep sub-micron technologies. Thus, parasitics derived from these tools can be off by 30% due to boundary cut errors and extraction rule sets which cannot possibly account for complex 3D effects accurately. NET-AN employs a fully seamless 3D Laplace/Poisson field solution using the fast proprietary "Cheetah II" solver to extract distributed RCLK models for specified nets. NET-AN will extract average IC clock nets in just minutes on popular workstation platforms. The "Cheetah II" 3D field solver achieves super linear performance through OEA proprietary algorithms which are unparalleled in the industry. Thus, solution times are kept to the absolute minimum without resorting to less accurate approximation methodologies.

Fully Coupled 3D Field Solution Parasitic Extraction

Multi-net simulations produce fully capacitively coupled and optionally inductively coupled distributed RCLM SPICE sub-circuit models. Using these coupled models accurate cross-talk and signal integrity simulations can be accomplished.

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Easy Single or Multi-Net Specification
The net browser allows net selection and highlighting in a variety of ways, either by annotated name, by selecting the net(s) with the display and mouse, or by using a reference GDSII cell. Individual nets, lists of nets, or groups of coupled nets may be specified for extraction. Also, the surrounding net expansion area to be included in the field simulation can easily be specified.

Full Path SPICE Circuits Using LEF/DEF
When a path or tree consisting of many nets is specified, NET-AN can automatically include the referenced driver, buffer and load cell SPICE sub-circuits in the main SPICE output file and add the appropriate measure statements. This allows you to quickly use the NET-AN results in SPICE to calculate accurate delay and skew values in report or SDF formats.

Optional Synopsys PrimeTime Interface
For accurate timing closure a more accurate interconnect model is required. NET-AN/PT offers 3D accuracy of the interconnect all operating from within the PrimeTime interface. NET-AN/PT can backannotate single or coupled net parasitics into PrimeTime and optionally can initiate SPICE level simulations using 3D parasitics and gate-level subcircuits.

Connectivity Based Hierarchical Graphic Interface
Reading standard IC data, display of the layout, selection of nets, building 3D models, and graphic display of color-coded delays is accomplished with the most advanced and flexible IC graphics tool on the market today, Post-Layout WorkShop. You can read and display an entire hierarchical VLSI module from a GDSII or converted CIF format. Full connectivity is calculated, nets renamed, nodes assigned, and then can be saved in a hierarchical net database. Display variables such as colors, stipple pattern, layer priority and layer on/off display status are easily modified. Levels of the hierarchy can be toggled on or off and specified areas zoomed in and out of the display.

Easy Process and Device Technology Definition
Using the Post-Layout WorkShop menus, the process technology for the design is easily defined and saved for future use. The metal and dielectric thickness are defined as well as metal process bias values. Material properties important for accurate extraction such as dielectric constant and metal resistivities are also defined. NET-AN recognizes IC devices such as transistors, resistors, and capacitors through flexible device definition menus and stores the definitions with the process technology. Complex structures such as conformal dielectrics, multi-metal layers, and local interconnect are easily defined.

Batch or Interactive Graphics Interface
NET-AN allows the freedom to operate either in a scriptable batch mode or a fully interactive graphics mode.

Other Related OEA Products

P-GRID - A power network analysis tool that extracts power network parasitics and solves them for low voltage violations and current density violations.

P-PLAN - A VLSI power distribution network floorplanning tool used with P-GRID for optimizing the geometric configuration of VDD and VSS rings, internal power rails, and ring voltage source pad locations using estimated block current sources.

CELL-AN - A three-dimensional level SPICE extraction tool that generates a cell or macro sub-circuit with significant RC, S/D resistances, and geometry dependent transistor SPICE model parameters.

BUS-AN - A tool for exploring the design space of a process technology as it relates to interconnect design limits and interconnect behavior. BUS-AN performs a variety of pre-design explorations such as inductive shielding effects, buffering strategies, clock-tree prototyping, and process corner simulations.

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