"NET-AN" a FULL THREE-DIMENSIONAL PARASITIC INTERCONNECT DISTRIBUTED RLC EXTRACTOR for LARGE FULL CHIP APPLICATIONS

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- Haris Basit - Rockwell International Corp

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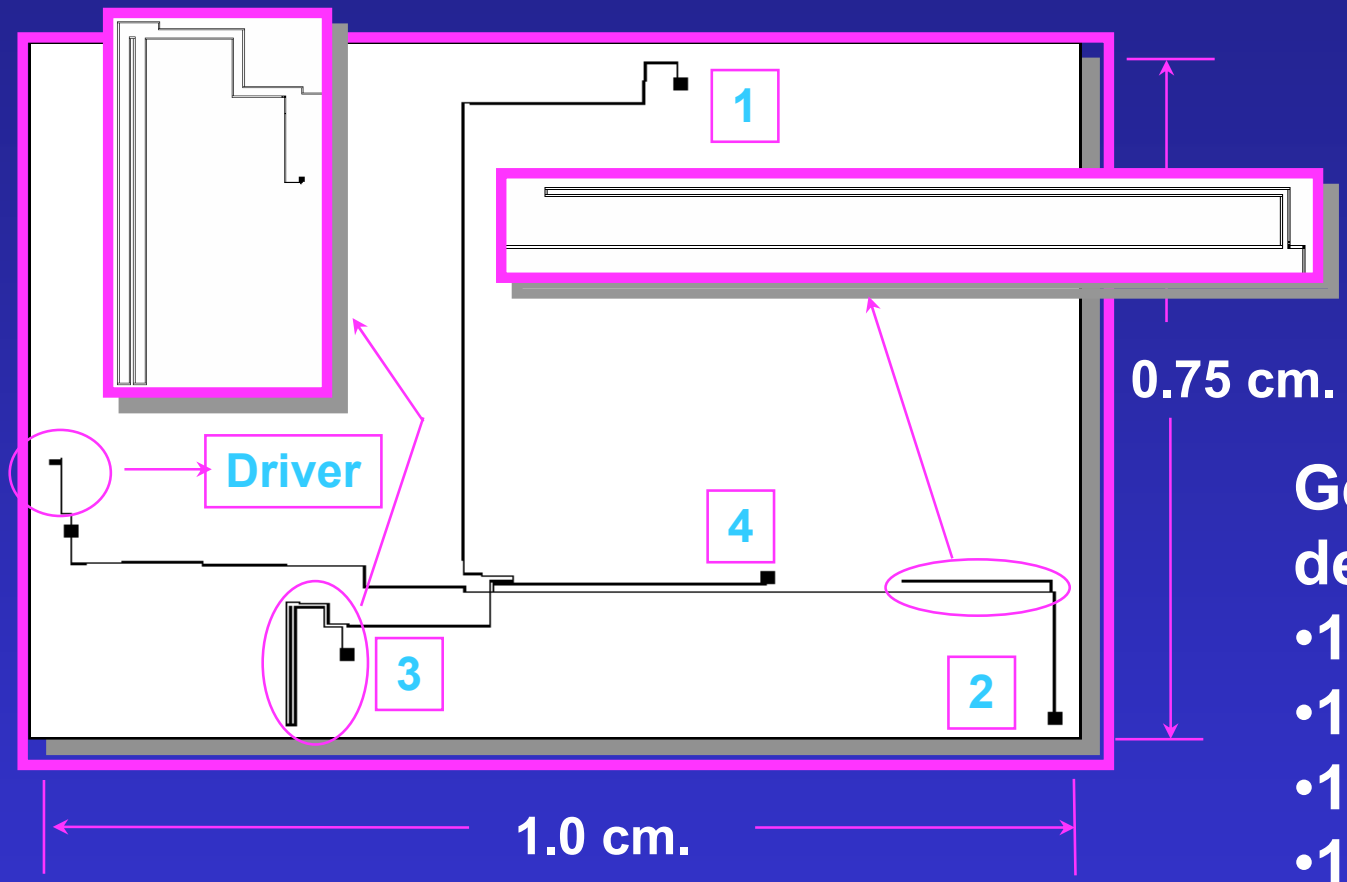
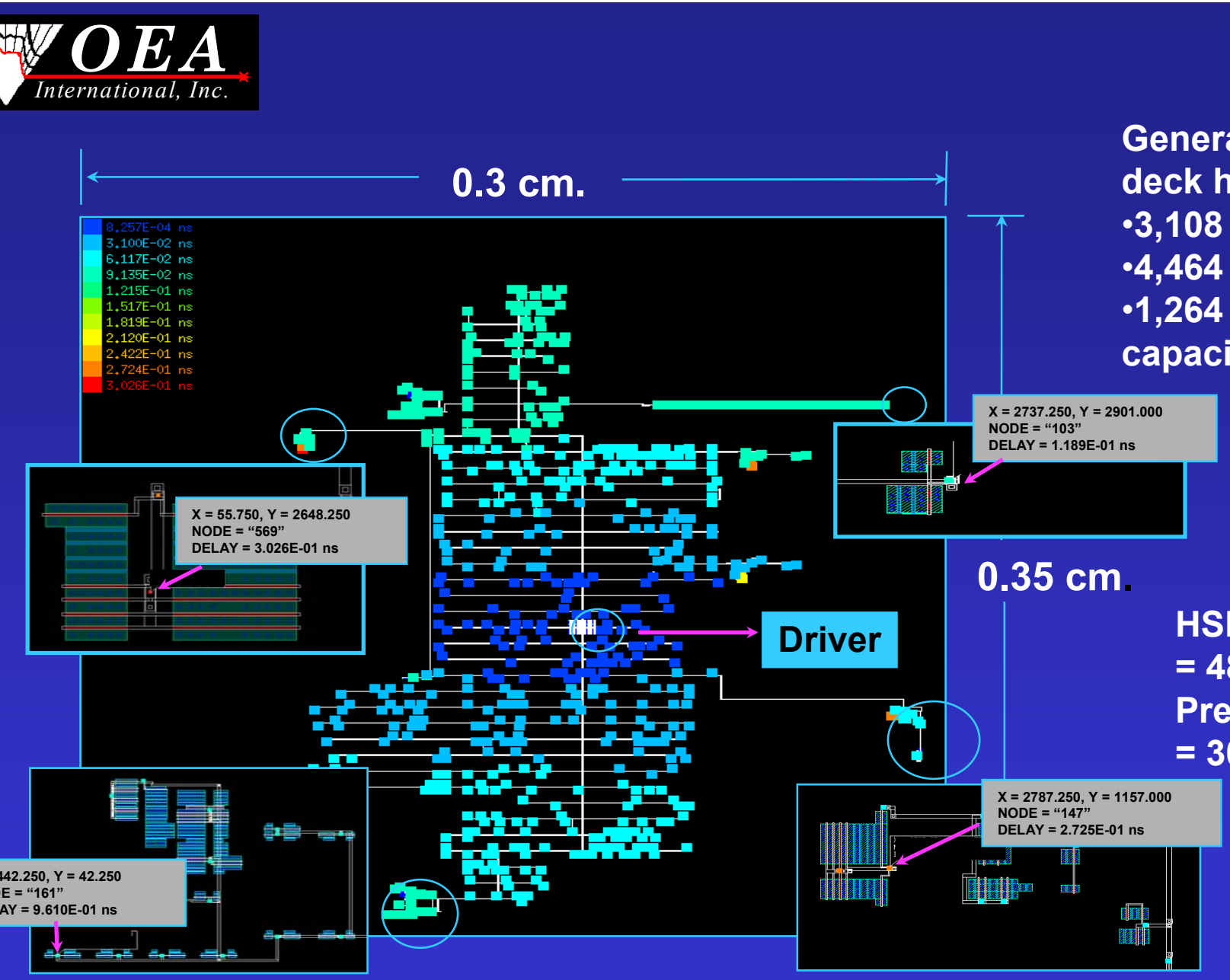


Level 1 Clock Net for a Major Microprocessor Chip

Generated spice deck

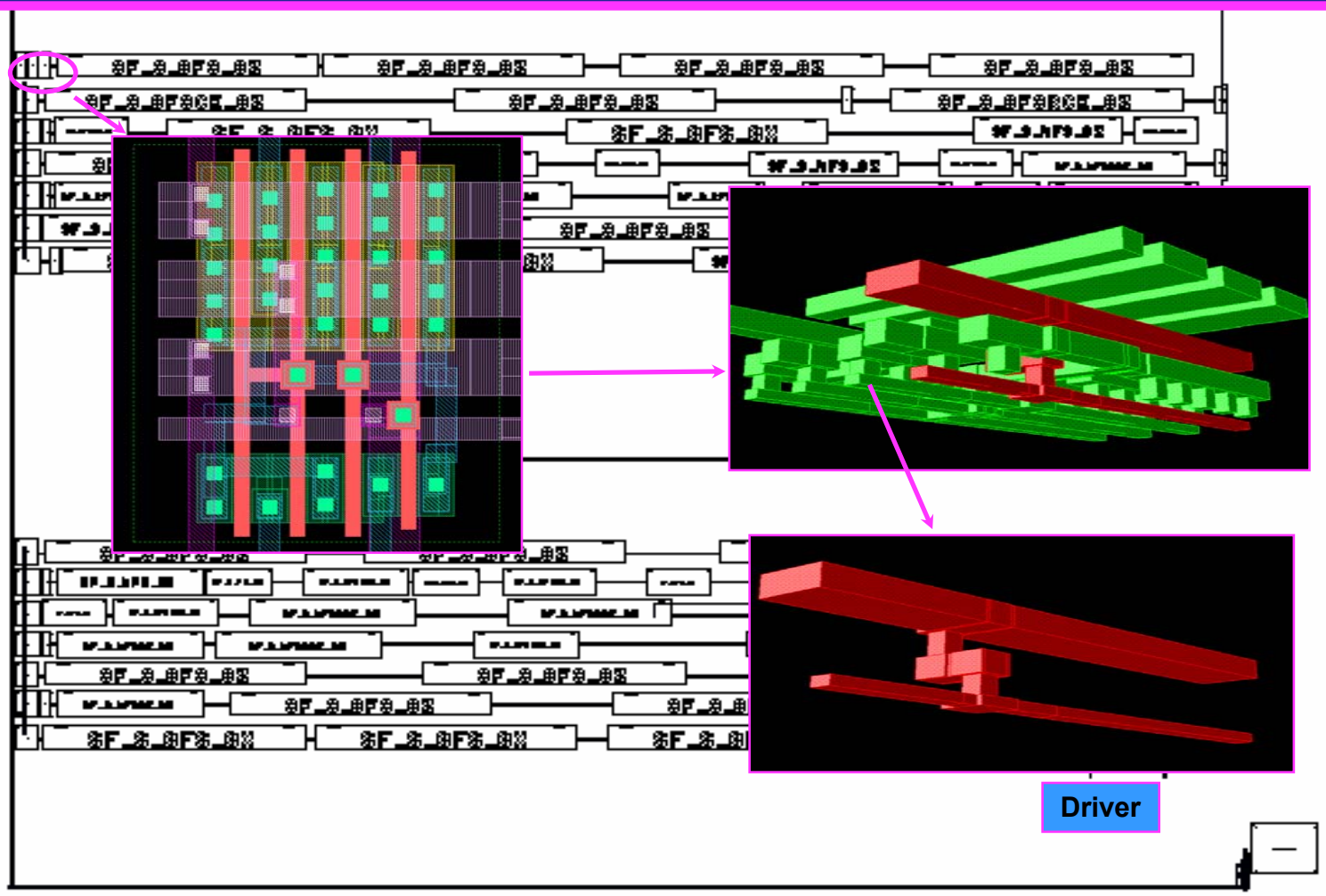
- 1,401 resistors
- 1,001 inductors
- 1,084 capacitors
- 16 gate capacitance loads



Generated spice deck has
- 3,108 resistors
- 4,464 capacitors
- 1,264 gate capacitance loads

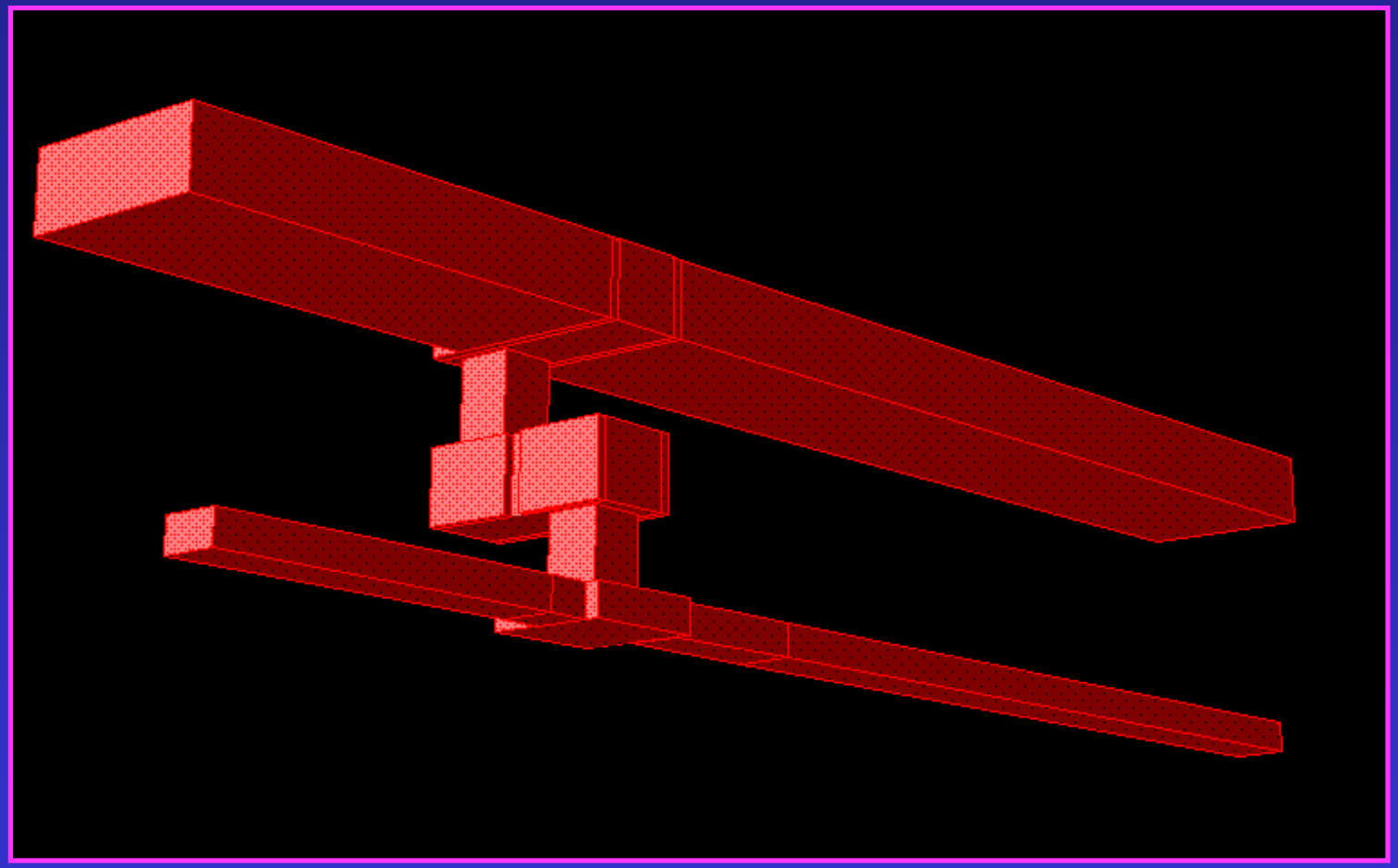
HSPICE runtime = 480 sec
Predicted skew = 301 pS

Level 2 Clock Net for a Image Compression Chip

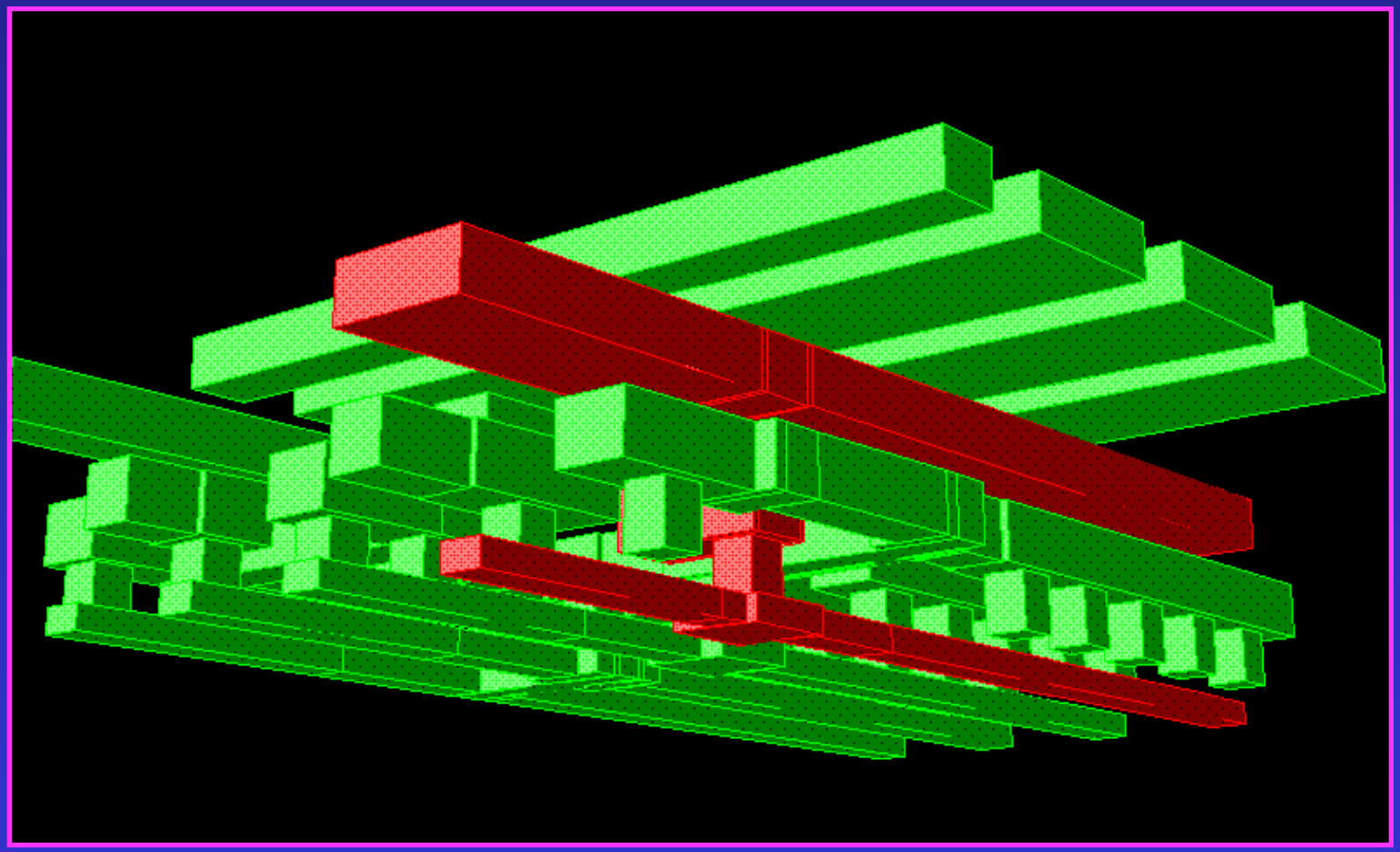


- 270 Clock Nets
- 102 Active Spice Circuits
- Spice Simulation 5 hours
- Extraction time hours

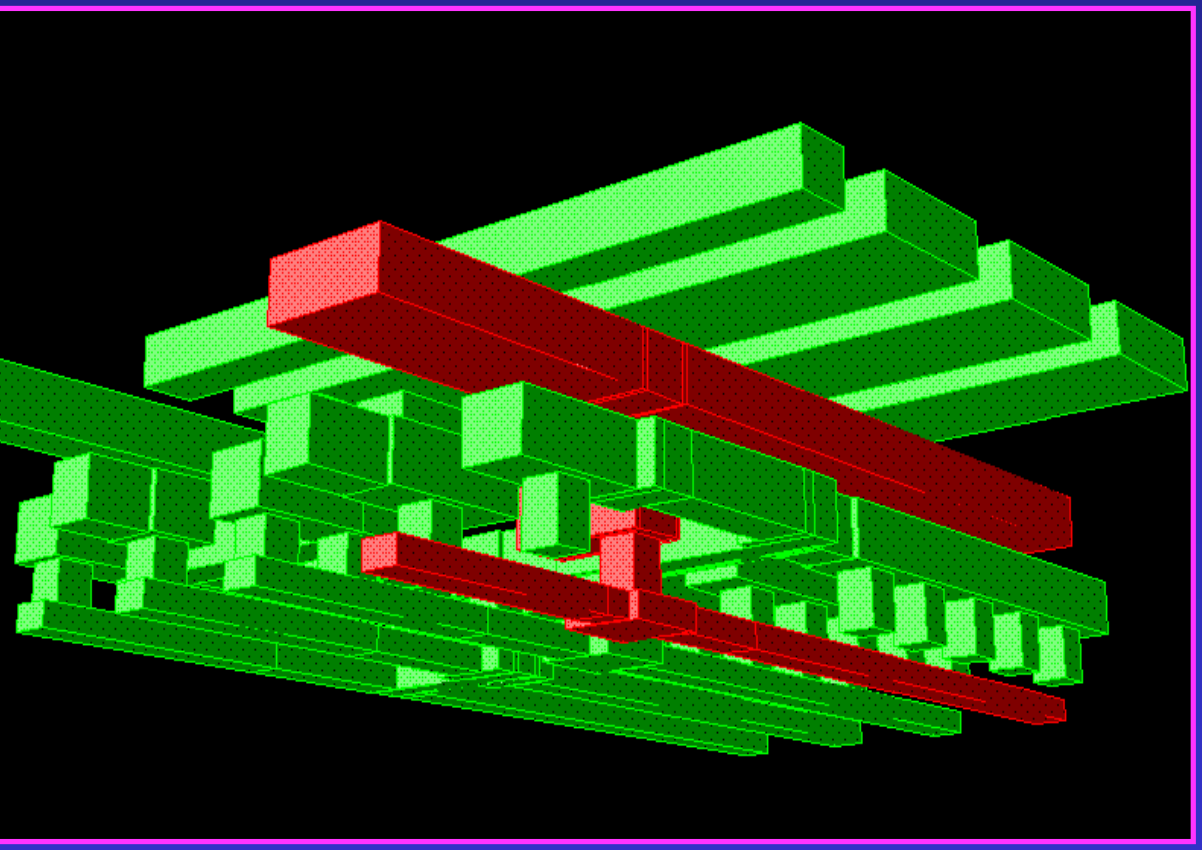
Level 3, 4 & 5 Clock Net for a Major Microprocessor Chip



3D View of Section of Selected Net



3D View of Section of Selected Net with Surrounding Nets



$$C = Q / V$$

$$\nabla(\varepsilon\nabla V) = \rho$$

$$\vec{E} = -\nabla V$$

$$\vec{D} = \varepsilon\vec{E}$$

$$Q = \iiint_{\Omega} \rho dv = \oiint_{\Gamma} \vec{D} \cdot d\vec{s}$$

Capacitance Calculation

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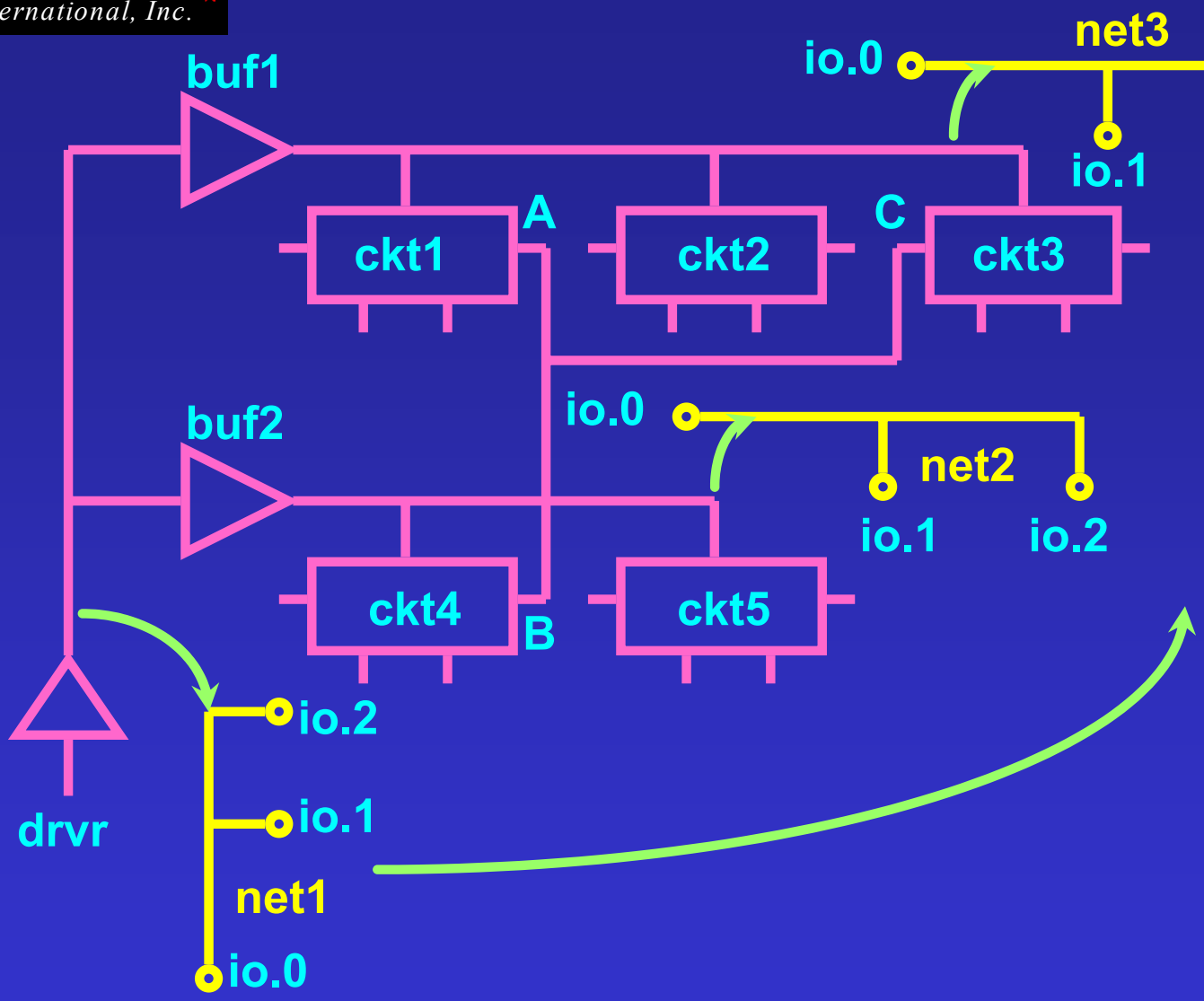
Single Net Subcircuit - net.master

```
.include net_sub.sp
.include source_cells -> defines
clocks
.include net_top.sp
.include net.gate_load
.include net.delay
.ends
```

Net Sub-circuits can be used individually or as part of a clock tree or critical path circuit

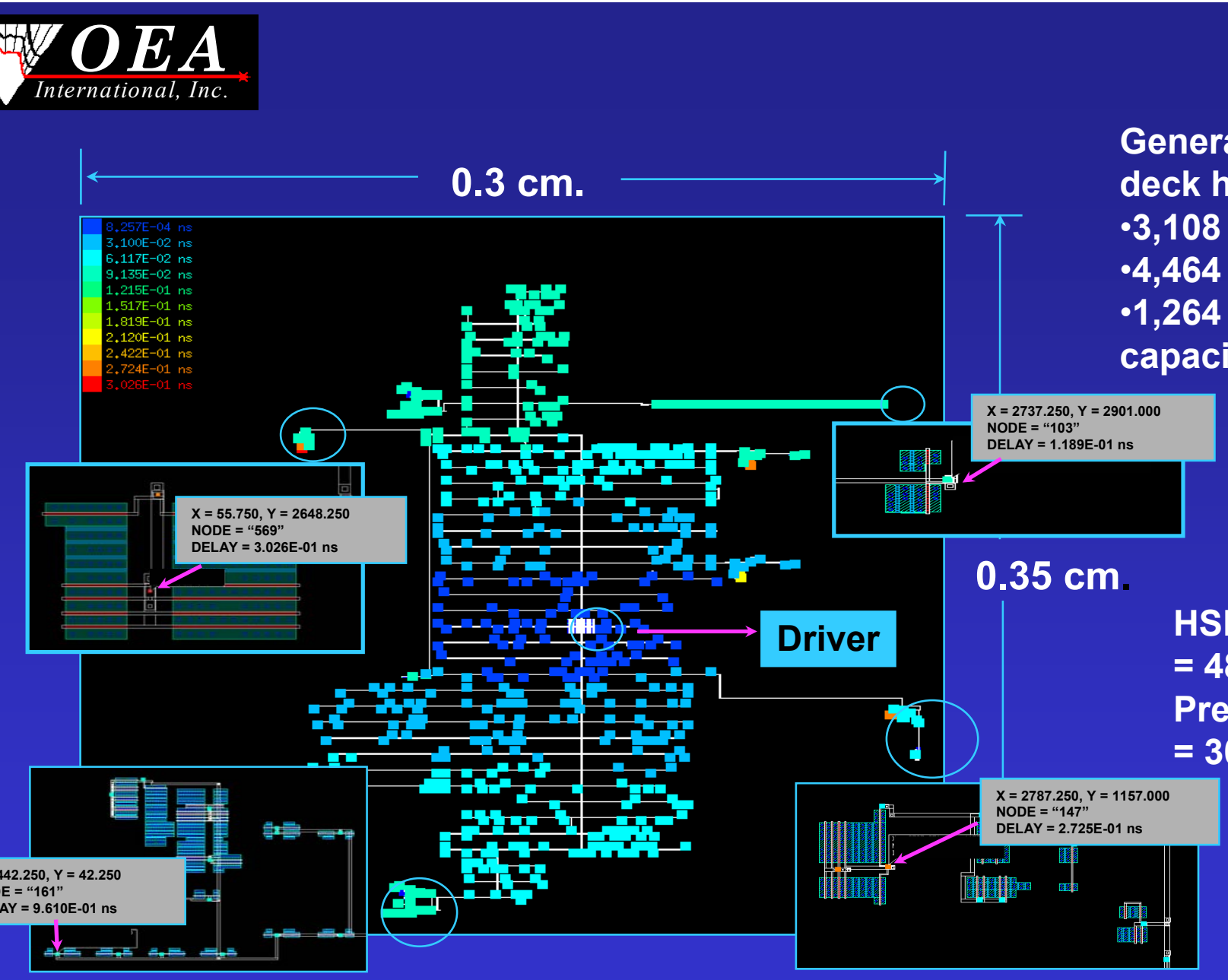
Multi-Net Clock Subcircuit - clk.master

```
.include net1_sub.sp
.include net1.top_name
.include net1_top.sp
.include net1.delay
.ends
.include net2_sub.sp
.include net2.top_name
.include net2_top.sp
.include net2.delay
.ends
.include net3_sub.sp
.include net3.top_name
.include net_top.sp
.include net.delay
.ends
```




```
.include net1_sub.sp
.include net1.top_nan
.include net1_top.sp
.include net1.delay
.ends
.include net2_sub.sp
.include net2.top_nan
.include net2_top.sp
.include net2.delay
.ends
.include net3_sub.sp
.include net3.top_nan
.include net_top.sp
.include net.delay
.ends
```

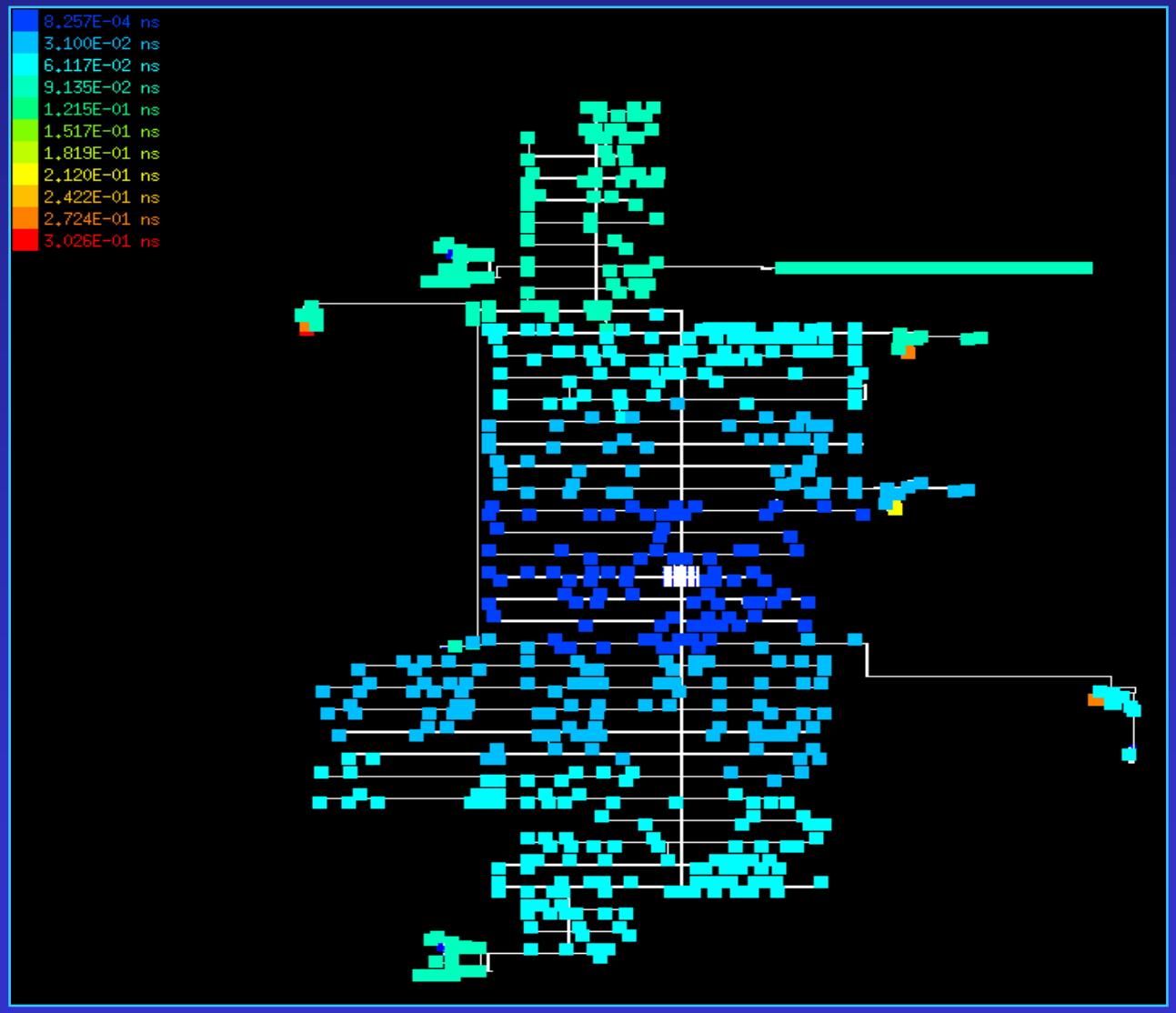
Clock Tree or Critical Path Spice Deck Generation



Generated spice deck has
- 3,108 resistors
- 4,464 capacitors
- 1,264 gate capacitance loads

HSPICE runtime = 480 sec
Predicted skew = 301 pS

Level 2 Clock Net for a Image Compression Chip



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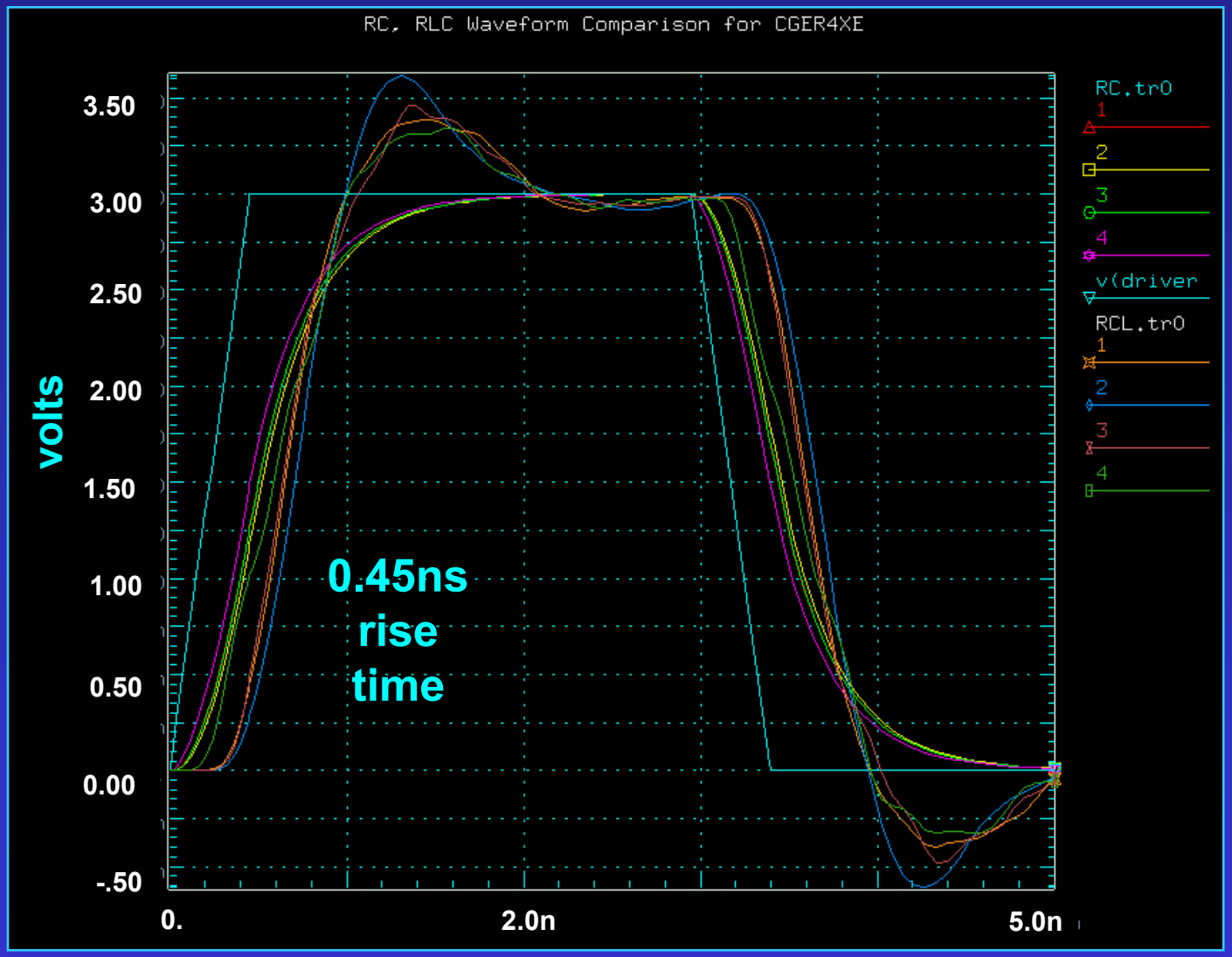
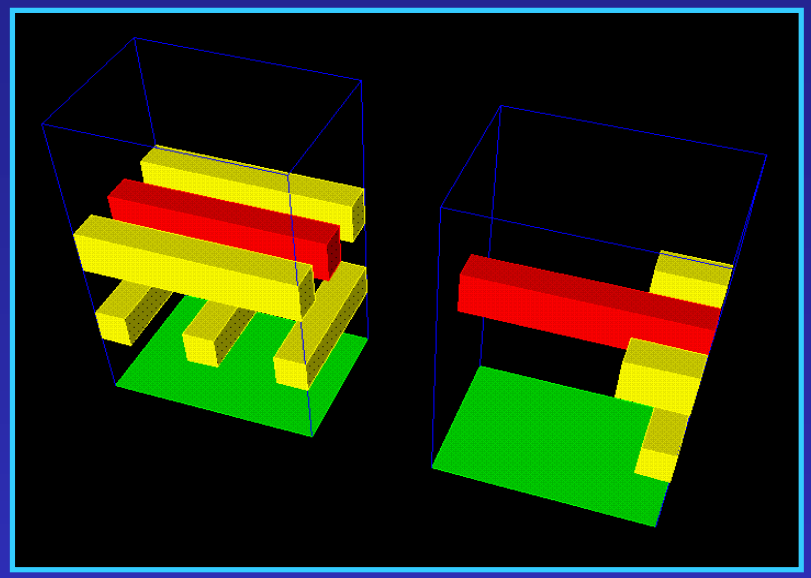
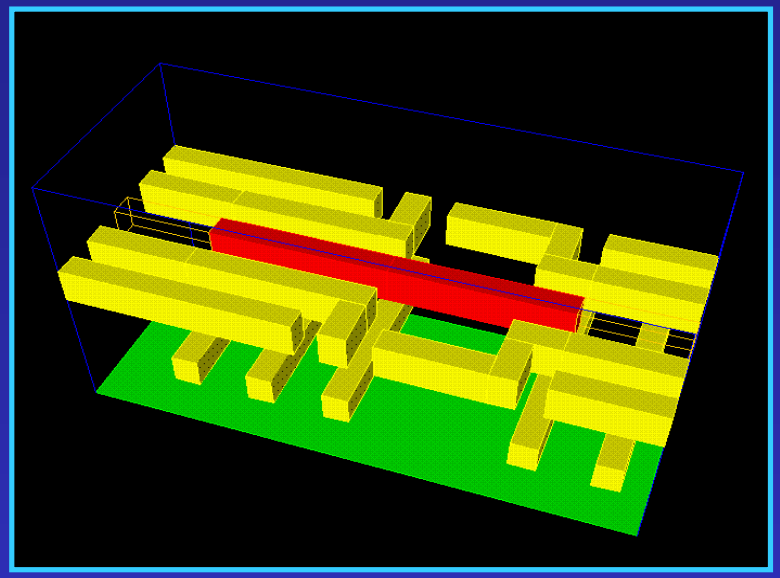
Color Coded Delay after Net-An Simulation



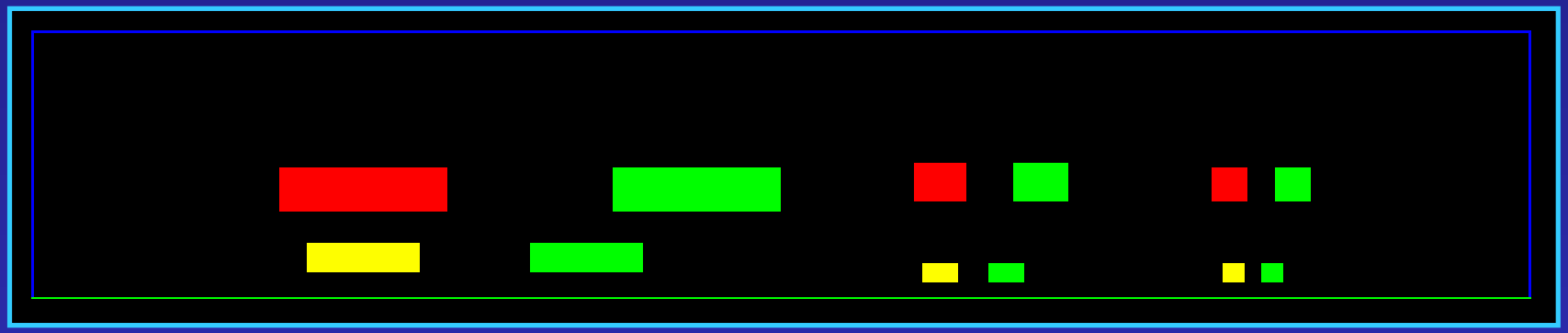
Comparison of Wave Forms with & without Inductance





	Cut & Paste Method			Full 3D Method	Cut & Paste Method Error	Full 3D Method	Cut & Paste Method Error
	Sect 1	Sect 2	Both				
Window	1 μ	1 μ	1 μ	1 μ		2 μ	
C11 full	0.847	0.443	1.290	1.413	9%	1.725	25%
C12	0.847	0.400	1.247	1.393	11%	1.705	27%
C11 gnd	0.001	0.043	0.044	0.020	120%	0.020	118%

Comparison of Full 3D Versus 3D Cut & Paste Extraction



	2μ	0.6μ	0.35μ
C11 fF	0.219	0.124	0.133
C12 fF	0.132	0.025	0.016
C12%	60%	20%	12%

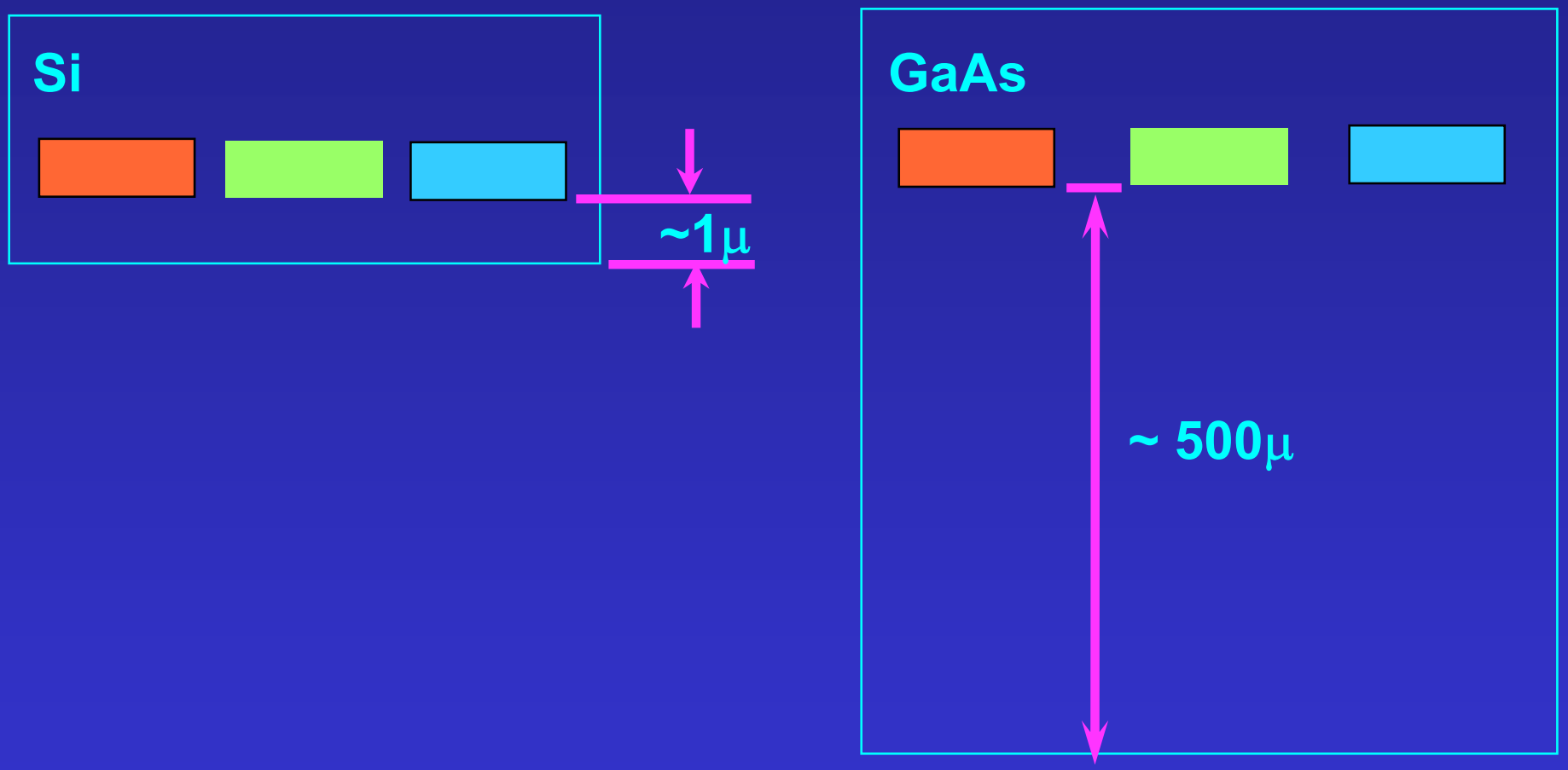
The Decreasing Significants of Parallel Plate Capacitance as Minimum IC Feature Size Decreases

	C(pf)	C_{true} (pf)	CPU Time (hrs)	Gate Load (pf)	# of Gates
Circuit 2	6.37	18.2	16.7	23.7	1264
Circuit 3	3.54	14.13	1.8	0.385	16

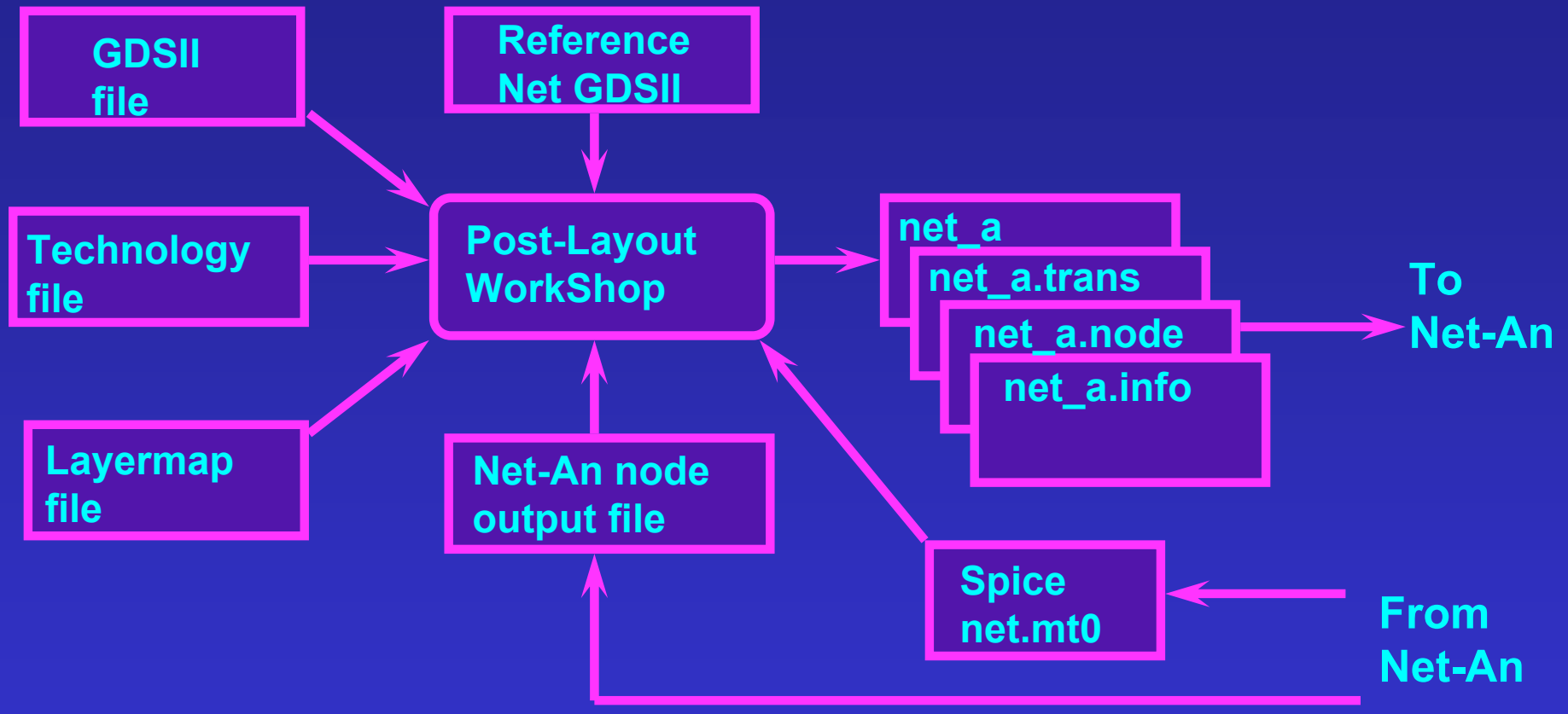
Effects of the Proximity Structures on the Net Capacitance

	T_{d1} (ps)	T_{d2} (ps)	T_{d3} (ps)	T_{d4} (ps)	Skew (ps)
RLC	422	479	410	360	119
RL(2*C)	640	732	619	539	193
RL(0.5*C)	278	315	270	248	67
RC	275	295	276	228	67
R(2*C)	499	543	500	404	139
R(0.5*C)	162	171	162	138	33
C	0	0	0	0	0

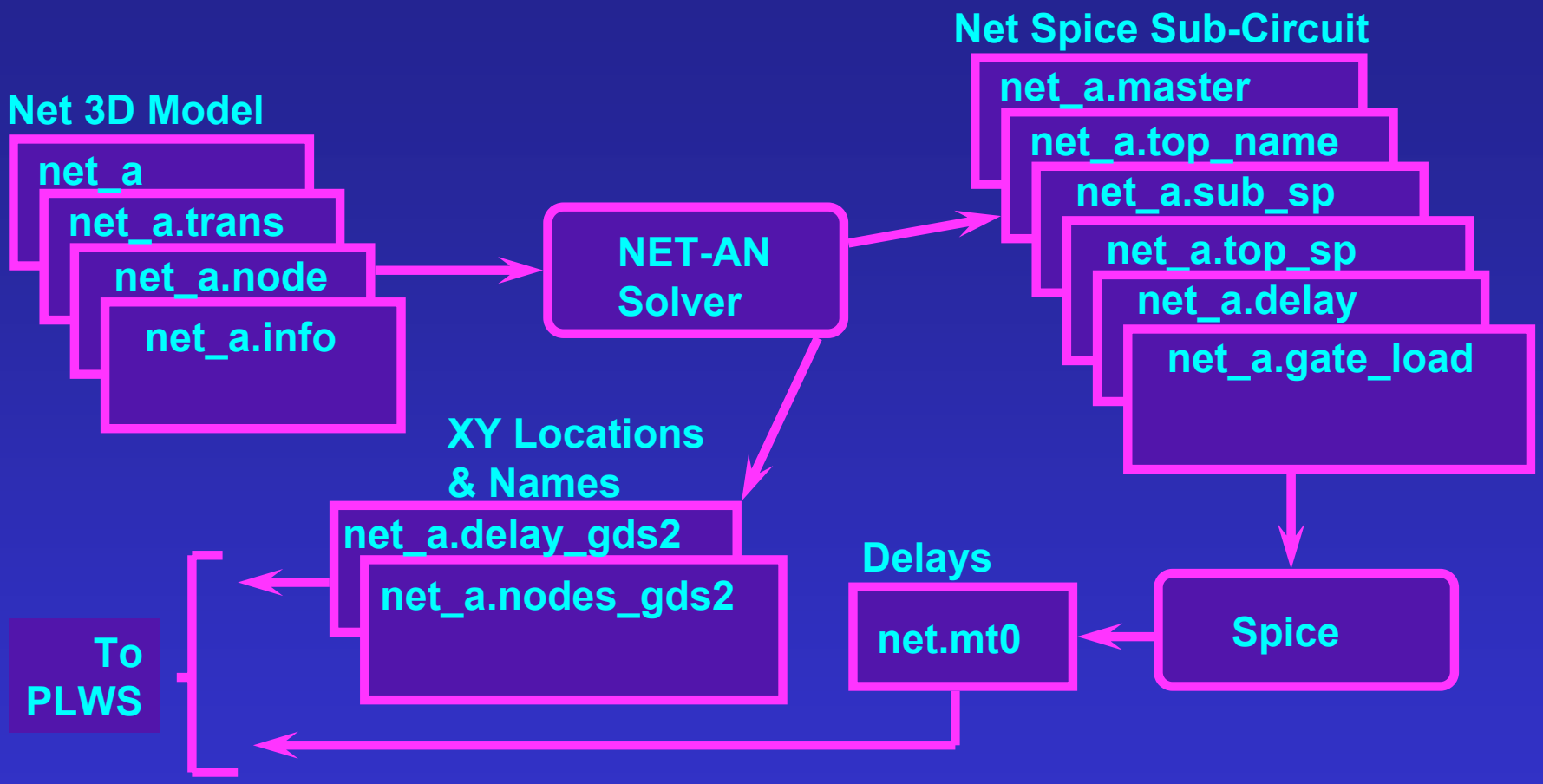
Delay and Skew Comparison for the Level 1 Clock Net for different model complexities and effects of under and over estimating the distributed capacitances.



Silicon vs GaAs Technologies



Net 3D Model Extraction Process



Net Parasitic Extraction Process

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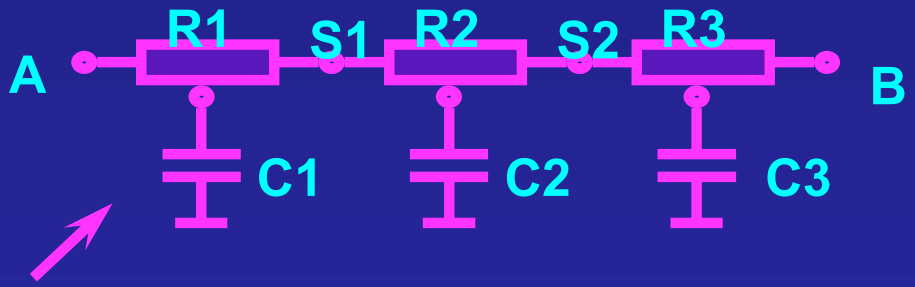
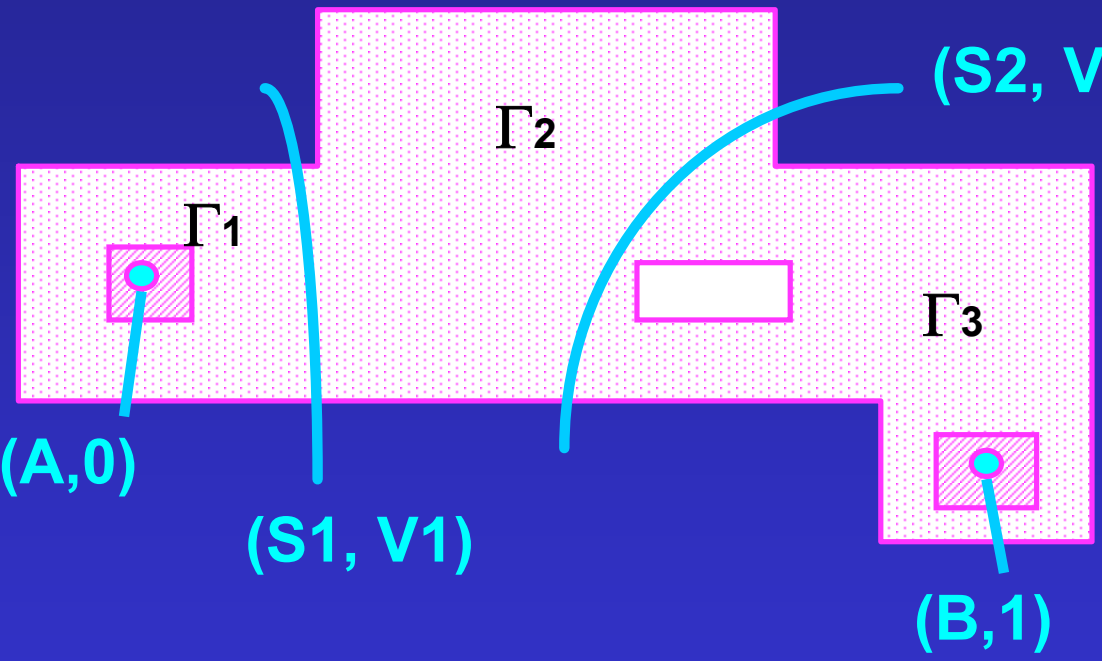




$$R = V / I$$

$$\nabla \vec{J} = 0$$

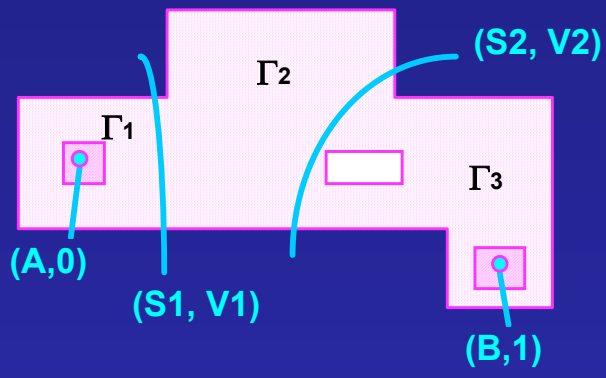
$$\vec{J} = \sigma \vec{E}$$

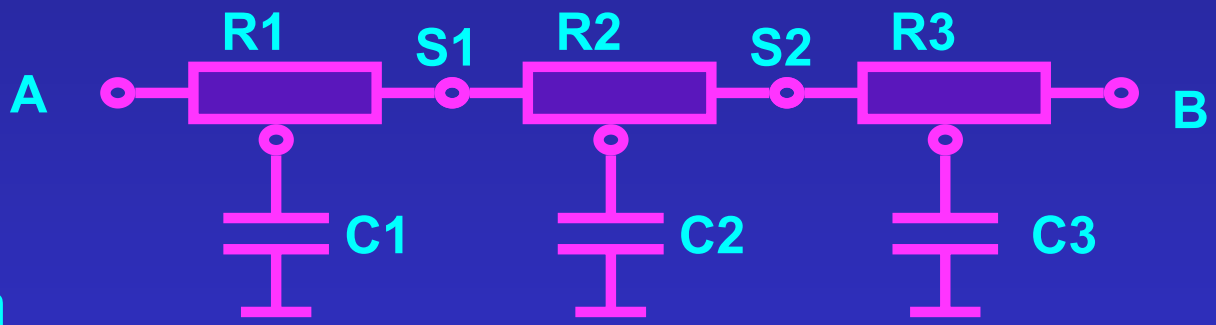
$$\vec{E} = -\nabla V$$

$$\nabla (\sigma \nabla V) = 0$$

$$I = \oiint_S \vec{J} \cdot d\vec{s}$$

Resistance Calculation



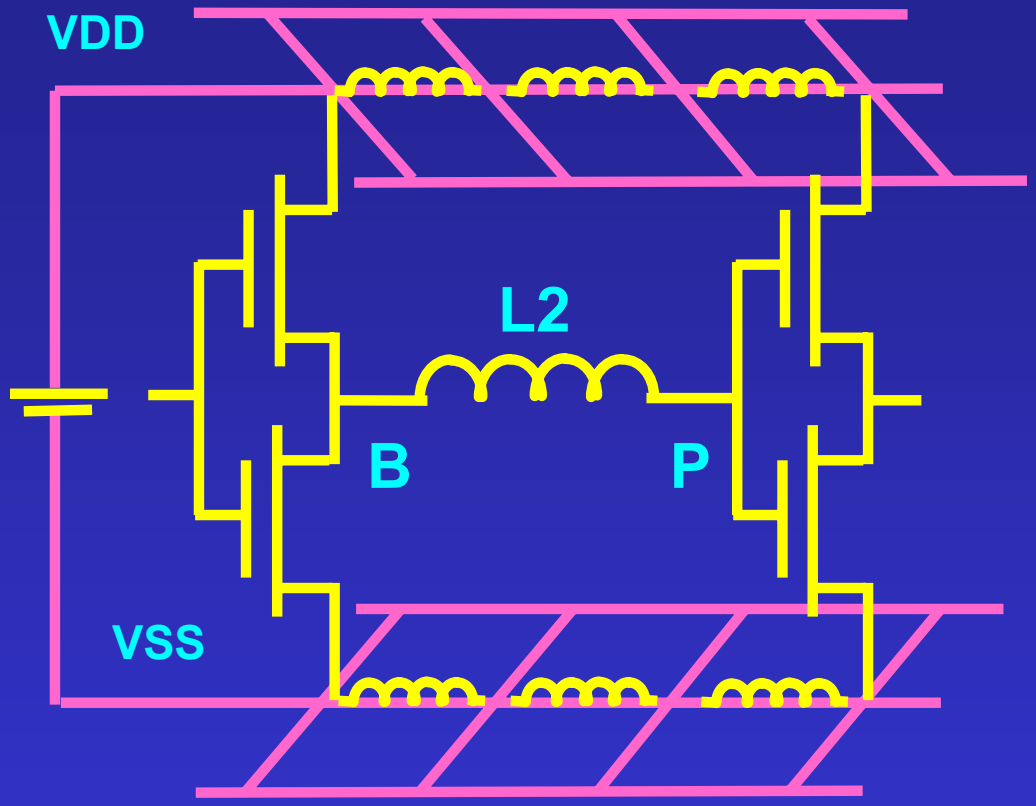


from

$$\nabla(\varepsilon\nabla V) = \rho$$

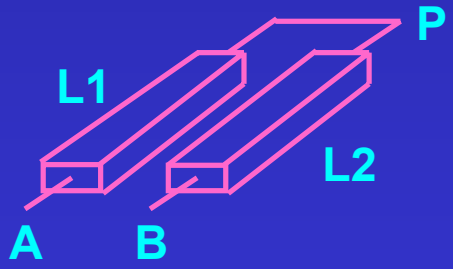
$$Q1 = \oint\!\!\!\oint_{\Gamma 1} \vec{D} \cdot d\vec{s},\quad Q2 = \oint\!\!\!\oint_{\Gamma 2} \vec{D} \cdot d\vec{s},\quad Q3 = \oint\!\!\!\oint_{\Gamma 3} \vec{D} \cdot d\vec{s}$$

Calculating Capacitance of the Resistance Regions



$$L_{AB} = L_1 + L_2 - 2\,L_{12}$$

$$L_{BP} \overset{?}{\cong} L_1$$



Inductance Approximation

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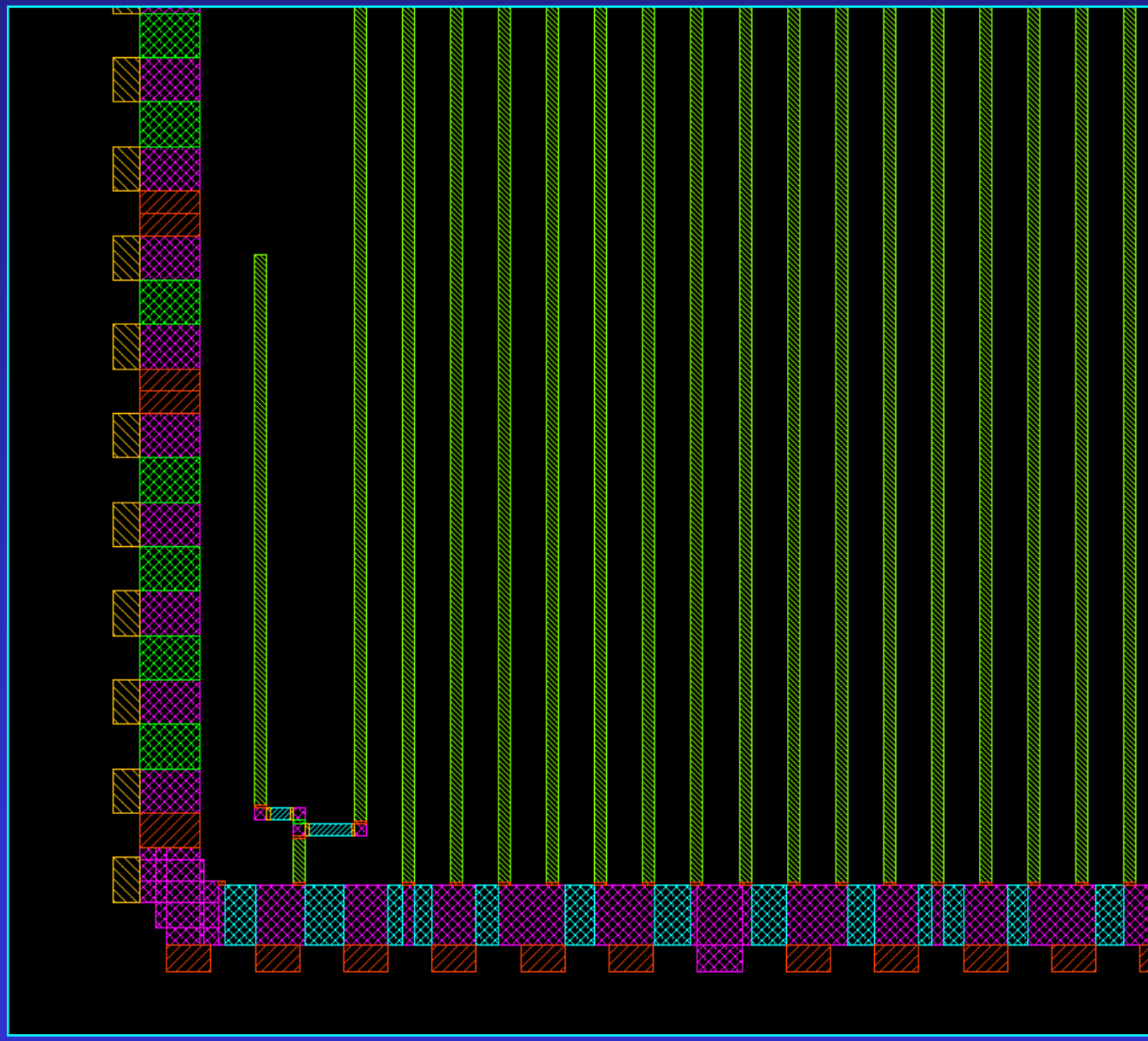
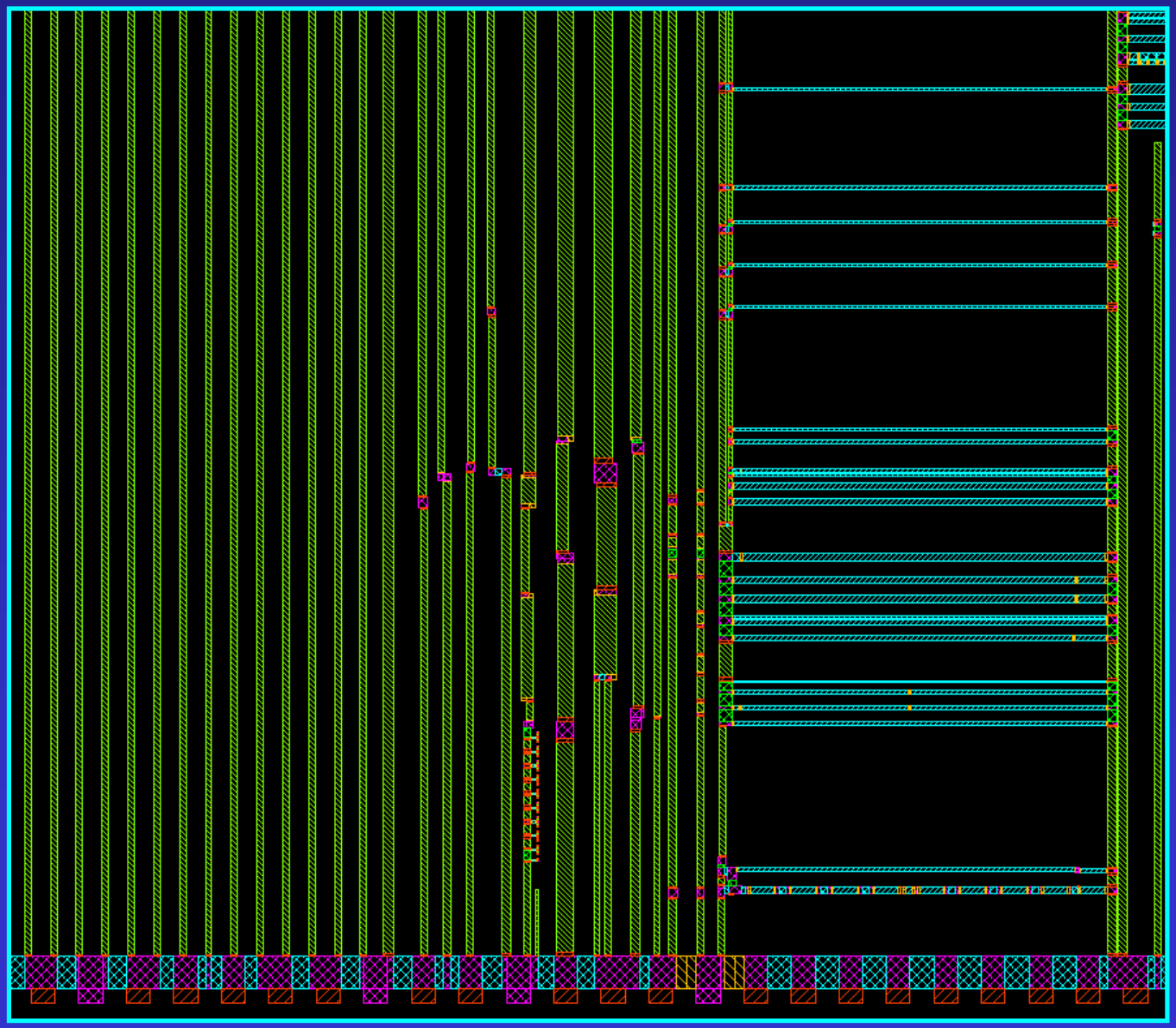
Detail of the Corner of the Power Grid



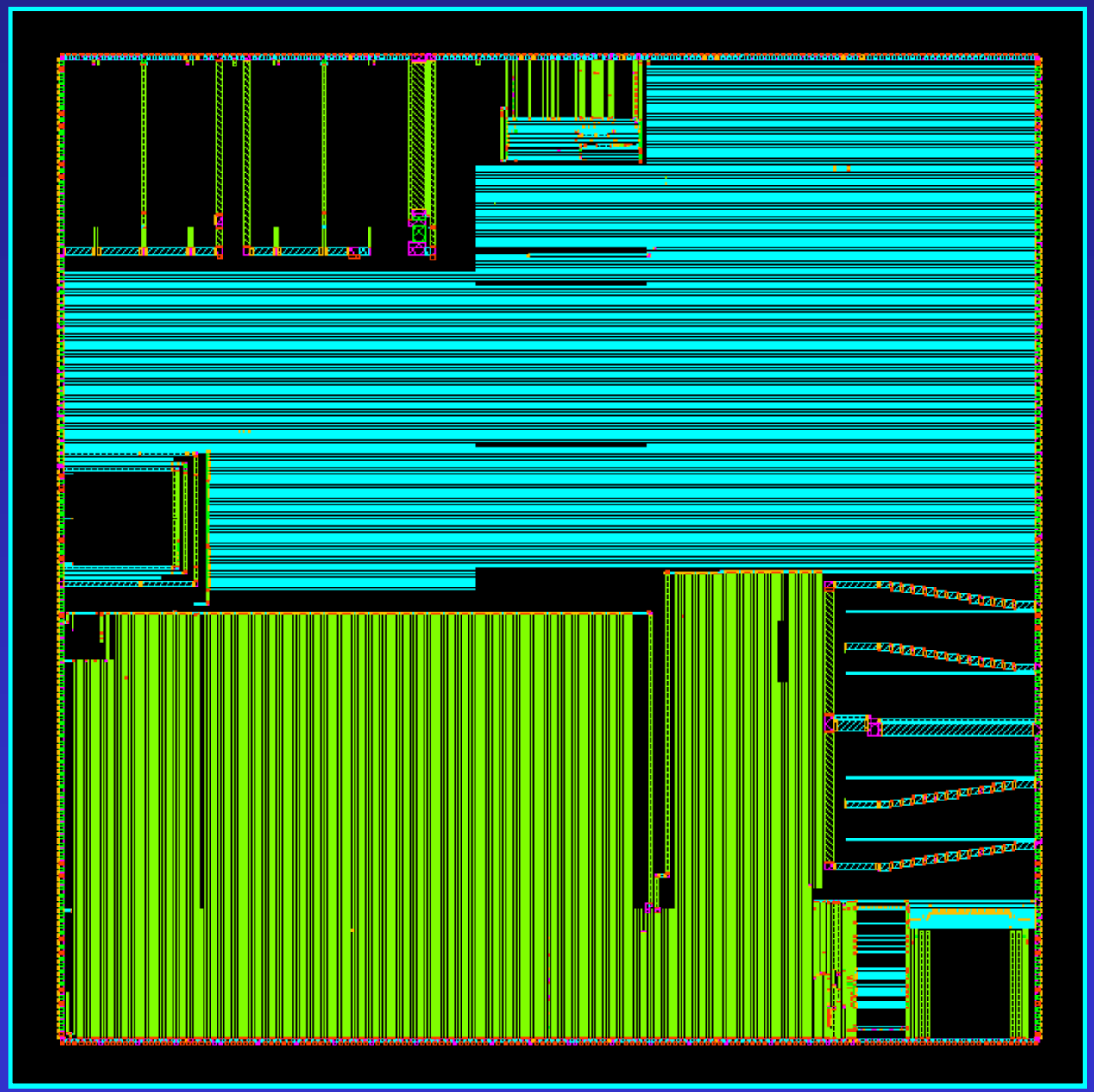
Detail of the Center Section of the Power Grid



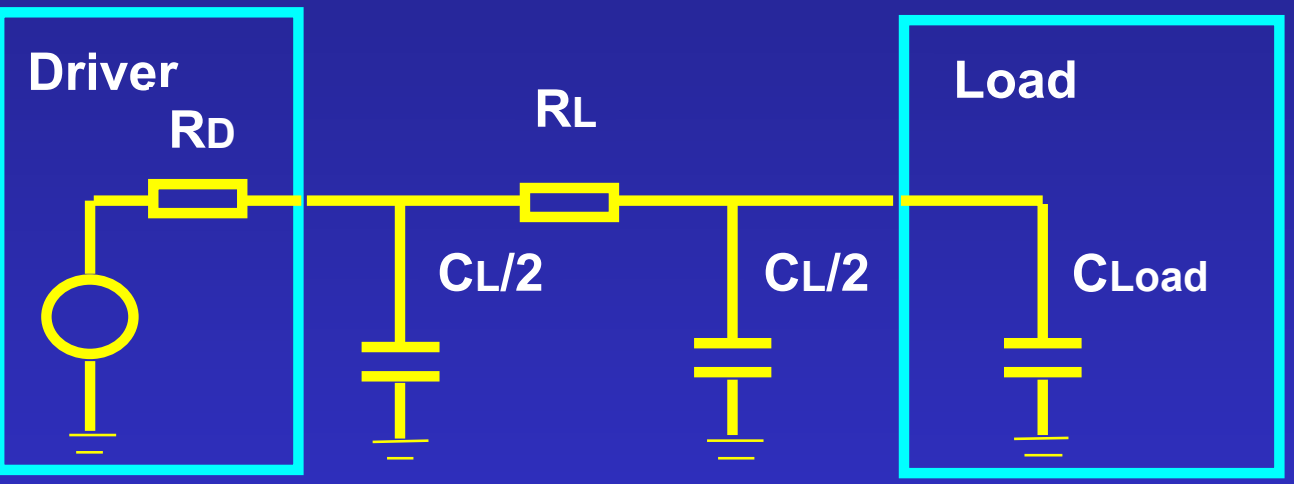
Full Chip Top Level VDD Net

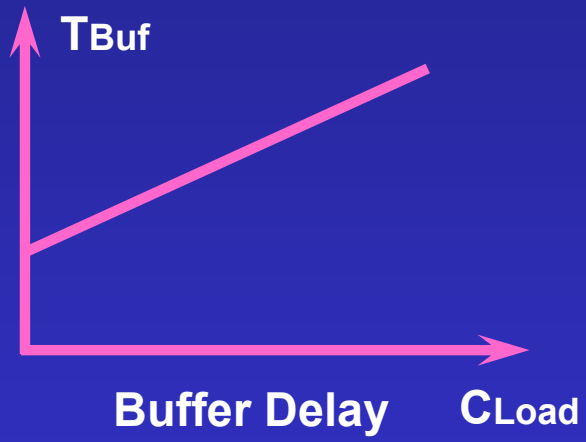
880,000 vias tied to last layer metal

40 MB GDSII File



Interconnect Delay Dominated Net Identification





$R_D * C_{Load} >> R_L * C_L$ Possibility NOT interconnect Problem

$R_D * C_{Load} <= R_L * C_L$ Interconnect Problem

R_L - Interconnect Resistance

C_L - Interconnect Capacitance

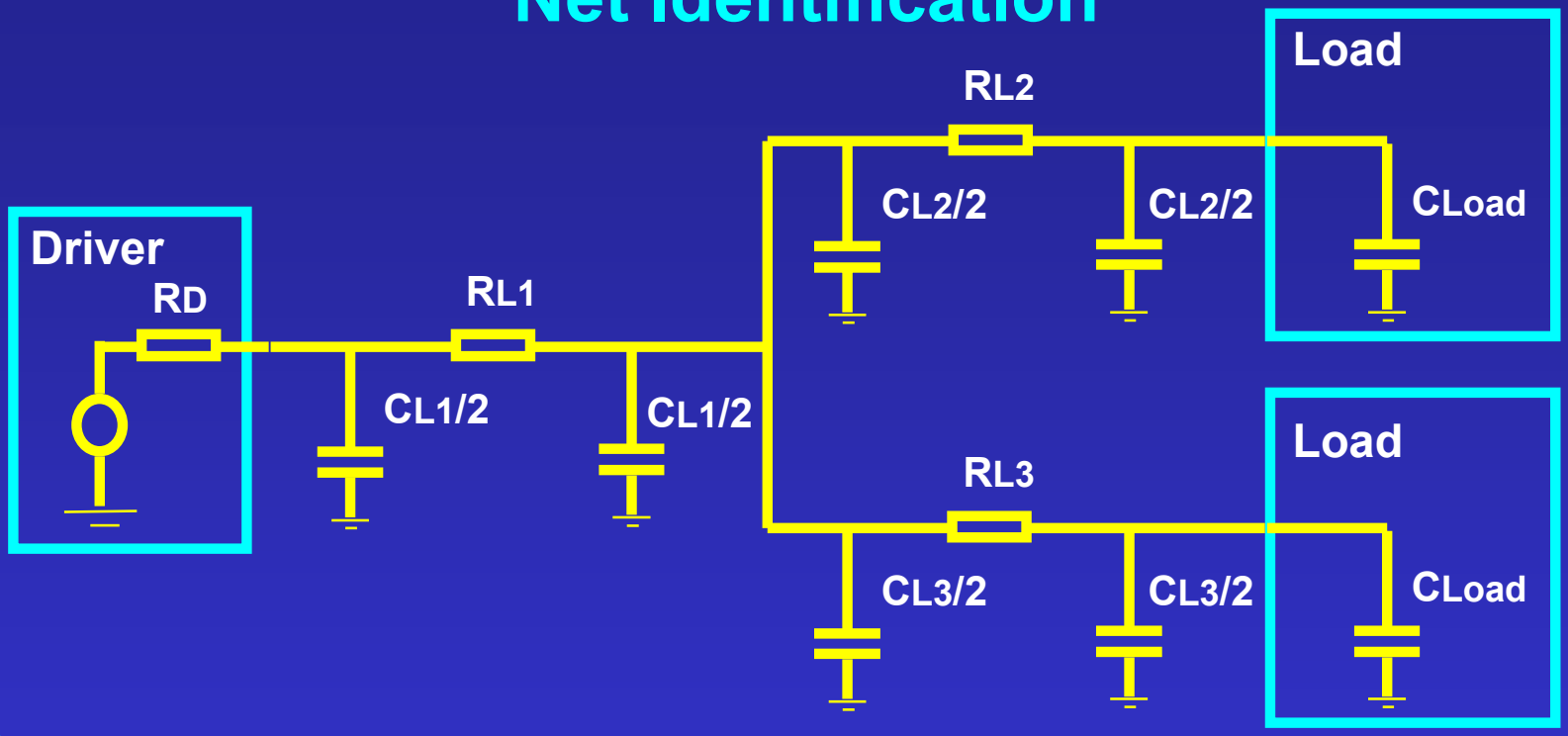
Agenda

- Interconnect Delay Dominated Net Identification
- Effects of Scaling of the Geometries on the Interconnect Capacitance
- Other Possible Alternatives
- Methodology Employed in NET-AN
- Usage
- Results and Conclusions

Conclusions

- A need for a 3D RLC extraction capability is shown for critical nets.
- Effects of possible RLC extraction inaccuracies on the delay/skew numbers are given.
- It is shown that it is possible to perform a full 3D RLC extraction for critical nets/paths on very large designs as an essential part of the design flow.

Interconnect Delay Dominated Net Identification



$R_D * \sum_{i=1}^{n} C_{Load_i} >> MAX\{R_L * C_L\}$ i=1,n — Possibility NOT Interconnect Problem

$R_D * \sum_{i=1}^{n} C_{Load_i} <= MAX\{R_L * C_L\}$ i=1,n — Interconnect Problem

R_L - Interconnect Resistance C_L - Interconnect Capacitance