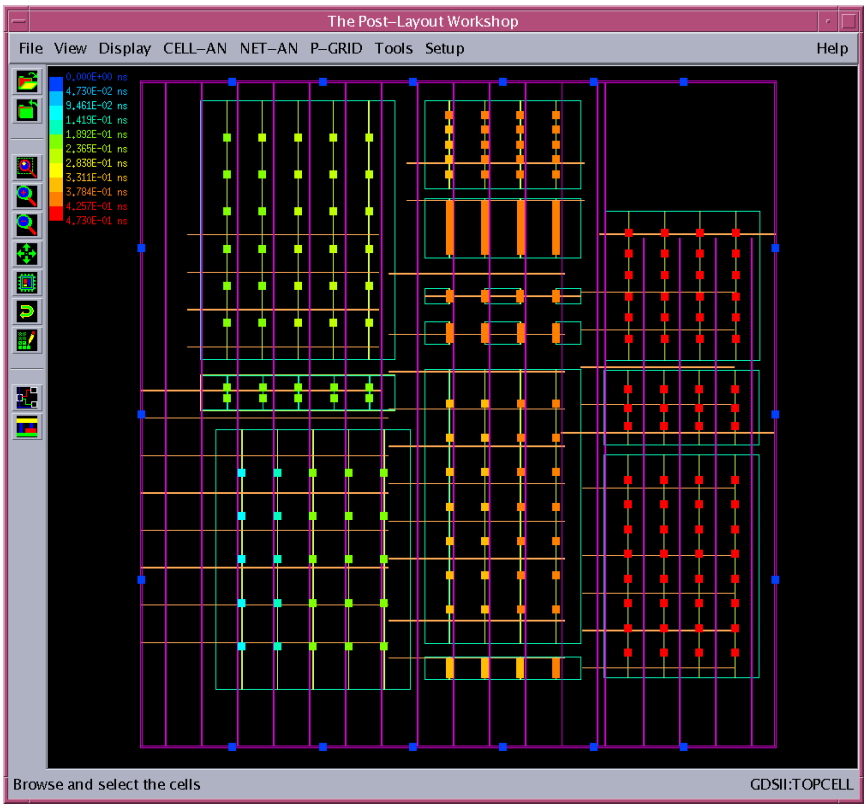
CLOCK Designer

VLSI Clock Floorplanning Tool



CLOCK Designer™ Features:

- *Complete fast full circle creation of planned clock layout, accurate extraction, circuit analysis, and color coded visual feedback*
- *Supports gridded, H-Tree, and Spine type clock routing strategies*
- *Works with OEA NET-AN to extract 3D RCLM parasitic network and SPICE to simulate accurate predictions of delay and skew*
- *Fast cycle time for quick what-if analysis to optimize clock network widths, spacings, and buffer locations*
- *Fast trade-off analysis of driver strength versus skew and/or power*
- *Runs on all popular workstation platforms*

CLOCK Designer is a VLSI floorplanning tool for the fast design and optimization of clock networks at the block or full chip level. The program allows for design using gridded, H-tree, or Spine routing strategies. CLOCK Designer can be used to perform a wide variety of what-if scenarios to minimize skew and eliminate delay failures. CLOCK Designer can eliminate days of redesign time due to poor planning of clock routing.

Fast Iteration Times

CLOCK Designer allows easy modifications to the planned clock network layout. Using an easy to modify input control file allows the user to try many alternative strategies and trade-off driver strength with line width and spacing alternatives. Also, the optimal driver and buffer locations can be easily determined to minimize skew and increase the performance of the chip design.

Full Creation, Extraction, SPICE Simulation and Feedback Loop

Using the control file and a technology file, a 3D model of the clock network is created including all driver/buffers and loads. An accurate RCLM SPICE sub-circuit of the interconnect is extracted using OEA NET-AN 3D extractor. Then, load and drivers are added, measure statements are included and the full circuit is simulated in SPICE to obtain delays, skew power and current consumption values. This data is then analyzed and the results presented in a report format and also loaded into the OEA PLWS graphic interface for color-coded viewing of the geometry and the predicted delays and skews.

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