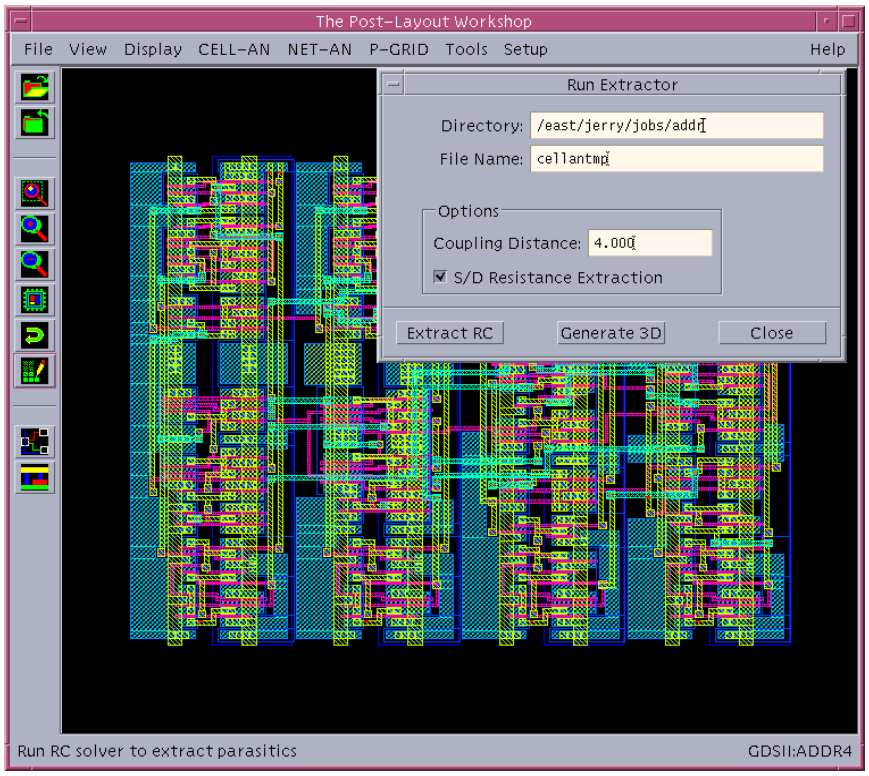
CELL-AN

3D Cell Field Solver SPICE Extraction Tool



CELL-AN™ Features:

- ***Utilizes fully seamless 3D field simulation solver to output highest accuracy, fully coupled, RCLM cell sub-circuits***
- ***Cell SPICE extraction including all layout dependent MOS transistor parameters***
- ***Utilizes full field simulation for accurate source and drain resistance on complex structures***
- ***Optionally accounts for above-the-cell routing effects***
- ***Push-button graphic interface or batch operation***
- ***Runs on all popular workstation platforms***

Today's deep sub-micron technologies require precise 3D RC extraction tools for operation of SPICE sub-circuits. For this reason one or two dimensional formula-based extraction tools which may give capacitance and resistance results that are inaccurate by 30% or more can no longer be relied on. Transistor source and drain configurations have also become much more complex, to the point where simple square count methods for resistance calculations no longer applies and a full field solution method is required. CELL-AN employs a fully seamless 3D Laplace/Poisson field solution using the fast proprietary "Cheetah II" solver to extract distributed RC netlist for the entire cell geometry at one time. CELL-AN is the first and only cell SPICE extraction tool to deliver an accurate full 3D capacitance and resistance extraction, a patented field solution source and drain resistance calculation, and a transistor geometric parameter extractor for a one step cell or macro cell SPICE deck generation capability.

Extracts Accurate 3D RC

CELL-AN utilizes the proprietary Cheetah II solver technology for fast and accurate seamless full 3D field simulation of capacitance and resistance of the cell interconnect technology. CELL-AN is capable of handling large macro cell designs easily. Since the user can also define capacitance coupling and minimum resistance thresholds, the size of the SPICE file is controlled, and therefore further SPICE reduction is not required. Models can be defined as lumped C, fully distributed RC, RCL or RCLM.

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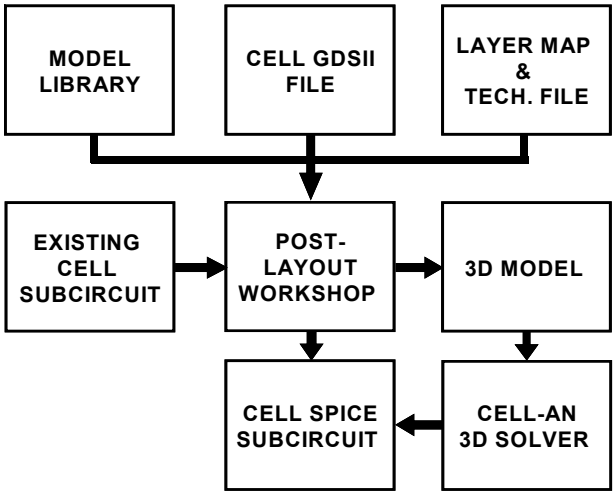
MOS Transistor SPICE Model Generation
CELL-AN automatically generates all geometry dependent MOS transistor SPICE parameters for inclusion in the full cell SPICE deck. Accurate source and drain resistances are automatically calculated using a proprietary field simulation methodology. Very complex single and multi-transistor configurations can be handled easily including contact-less regions, split gates, and honeycomb transistor structures.

Above the Cell Routing Effects
For designs which above-the-cell routing is possible, the user can define density factors for top level routing layers and phantom routing layers which will automatically be created. By using these layers, more accurate capacitance values of cell routing can be achieved.

Connectivity Based Hierarchical Graphic Interface
Reading standard GDSII data, display of the layout, selection of nets, building 3D models, and graphic display of color-coded delays is accomplished with the most advanced and flexible IC graphics tool on the market today, Post-Layout WorkShop. Display variables such as colors, stipple pattern, layer priority and layer on/off display status are easily modified.



Easy Process and Device Technology
Using the Post-Layout Workshop menus, the process technology for the design is easily defined and saved for future use. The metal and dielectric thickness are defined as well as metal process bias values. Material properties important for accurate extraction such as dielectric constant and metal resistivity are also defined. CELL-AN recognizes all IC devices such as transistors, capacitors, and resistors through flexible device definition menus and stores the definition with the process technology. Complex structures such as conformal dielectrics, multi-metal layers, and local interconnect are easily defined.

Other Related OEA Products

METAL - A general purpose 2D/3D interconnect simulator for extracting RCL parasitics from interconnect structures. It features automatic mesh generation and refinement, and automatic SPICE sub-circuit generation.

NET-AN - A three-dimensional IC multi-net analysis tool for extracting distributed RCLM SPICE networks from critical IC nets.

P-GRID - A power network analysis tool that extracts power network parasitics and solves them for low voltage violations and current density violations.

P-PLAN - A VLSI power distribution network floorplanning tool used with P-GRID for optimizing the geometric configuration of VDD and VSS rings, internal power rails, and ring voltage source pad locations using estimated block current sources.

BUS-AN - A tool for exploring the design space of a process technology as it relates to interconnect design limits and interconnect behavior. BUS-AN performs a variety of pre-design explorations such as inductive shielding effects, buffering strategies, clock-tree prototyping, and process corner simulations.

HENRY - A three-dimensional simulator that calculates inductance and mutual inductance of interconnect and ground plane structures.

OEA International, Inc.

Distributed by:

155 East Main Avenue, Suite 110
Morgan Hill, CA 95037
Phone: (408) 778-6747
FAX: (408) 778-6748
Email: info@oea.com
http://www.oea.com