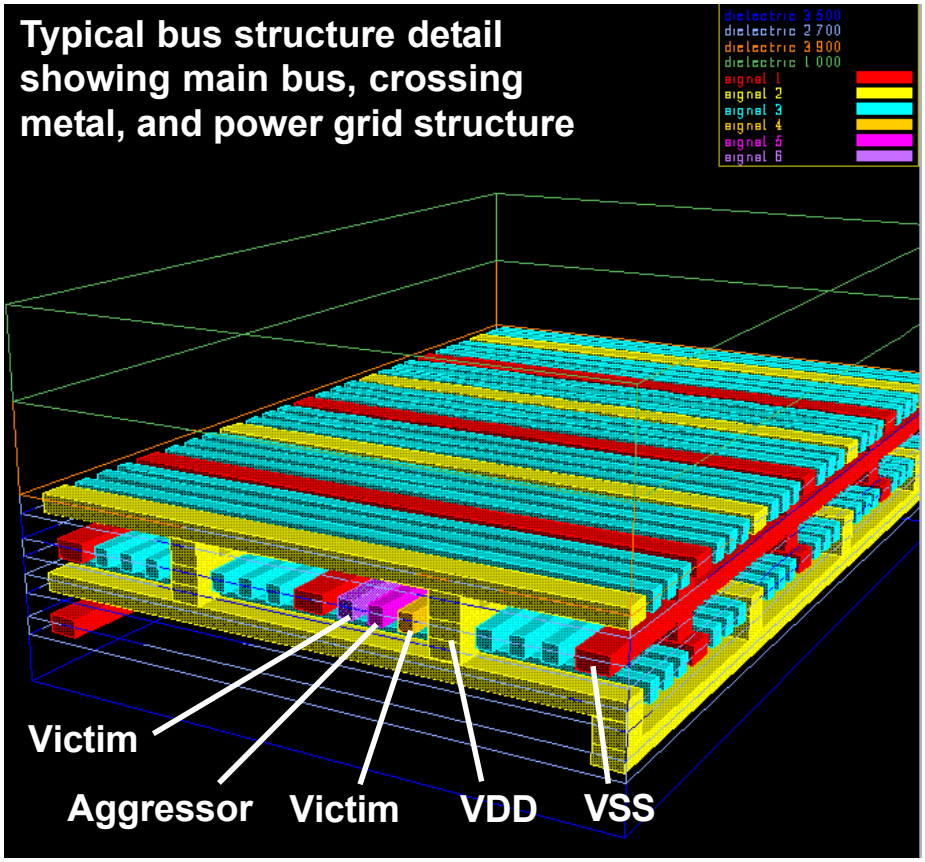
BUS-AN

Interconnect Design Planning Tool



BUS-AN™ Features:

- ***Prototype and Analyze Critical Nets and Buses in minutes***
- ***Full 3D modeling of RCLM parasitics using NET-AN™***
- ***Full Spice level simulation of driver/load cells and interconnects***
- ***Analyzes all possible drive and load combinations for optimum buffer selection***
- ***Hierarchical for Clock Tree Prototyping***
- ***Automated flow driven by simple control files***
- ***Runs on all popular workstation platforms***

The **BUS-AN** program is a powerful tool for exploring the design space of any foundry process technology as it relates to interconnect. With every foundry process and base cell library combination, practical interconnect design limits, interconnect delay and crosstalk behavior must be thoroughly analyzed. Using a technology file, an interconnect rules file, and your cell spice library **BUS-AN** can perform a variety of pre-design explorations:

- Evaluate tradeoffs in different routing line widths, spacing, shielding, and buffering strategies comparing them for overall skew and delay behavior.
- Evaluate a family of path segment files that may be of various lengths, widths, and/or spacing against a family of different drivers for delay and power tradeoffs.
- Evaluate a clock-tree fan-out strategy for predicted skew values.
- Evaluate numerous best-case and worst-case physical technology corners.
- Evaluate inductance and inductive coupling on buses and shielded clocks for delay, skew, crosstalk, and return path effects.
- Evaluate layer-to-layer inductive and capacitive crosstalk effects.
- Examine best-case and worst-case process variation effects quickly.

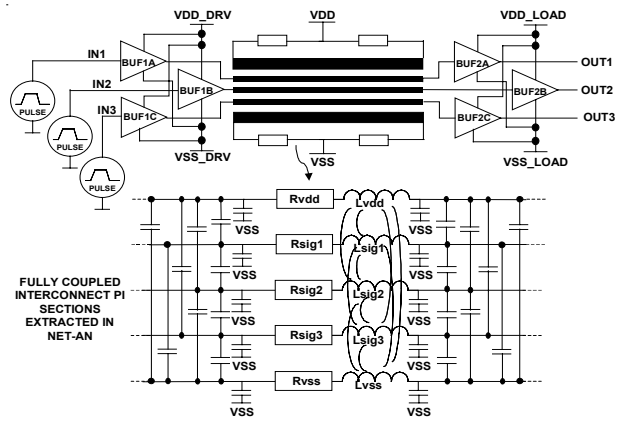
OEA International, Inc.

Easy to Automate Bus Geometry Creation

Since layout does not exist in the early design stages, **BUS-AN** creates all the necessary bus, shields, neighbors, and crossover layout automatically from simple descriptive statements in a control file and using a technology file. All node and nodal text is added and a GDSII file created to view the structures in schematic view/cross section view, and full layout view.

Accurate 3D Modeling of Bus Structure Parasitics

BUS-AN works in conjunction with the OEA **NET-AN** extraction software that employs the OEA proprietary "**Cheetah**" 3D critical net field solver. The solver performs a full seamless 3D field solution of the bus nets and surrounding defined geometry to yield a full RCLM distributed model of the interconnect. The **NET-AN Cheetah** solver is the fastest 3D field solver on the market. Using this solver guarantees the highest accuracy will be maintained in your results.



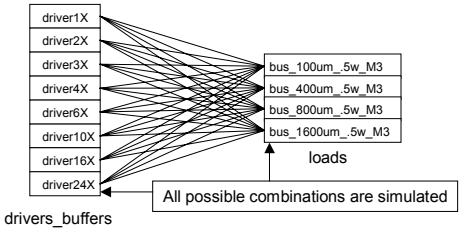
MULTI-SIGNAL BUS EXAMPLE WITH SHIELDS

Automatic Spice Master Simulation Files

A full analysis requires more than just geometry and an interconnect spice model. It requires a full top-level circuit with all of the drivers and loads attached and all of the measurement commands to output statistics on the simulation results. **BUS-AN** creates this file, error-free, saving the user hours of time creating and debugging hand-created master Spice decks. All of the pulses, includes, sub-circuit calls, run-time parameters, and measurement statements are automatically created by **BUS-AN**. Measurements are made for rise and fall delays, rise and fall slew rates, and min-ave-max-rms VDD/VSS voltages and currents for global and local nodes.

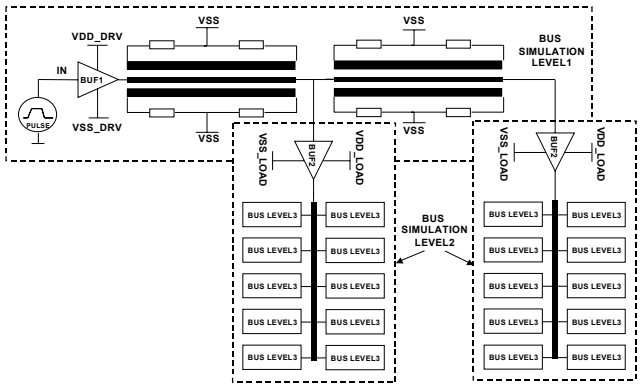
Automatic Detailed Driver/Load Family Analysis

A full N x M analysis can be done for buffer sizing versus different length bus structures on different metal layers. Plotted curves of current, power, delay, and skew can then be analyzed to find the best tradeoffs of line width, spacing, layer for different load sizes and driver/buffer sizes.



Hierarchical Clock Tree Strategies Easily Prototyped

BUS-AN allows levels of bus structures to be linked together making it easy to prototype any planned clock tree and multi-level bus hierarchical structure. All measurement data is automatically created to traverse the levels of hierarchy so delays and skews can be simulated from the top level drivers to all the loads on the bottom level.



CLOCK TREE EXAMPLE USING 2 LEVEL HIERARCHICAL BUS

Benefits:

- Eliminates costly layout, fabrication, and measurement of expensive test chips.
- Fully simulates realistic design rules early in the design process to avoid crosstalk problems, minimize skew and optimize speed.
- Allows a quick comparison of foundries.
- Allows optimization of buffering strategies for speed, power and chip space.

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